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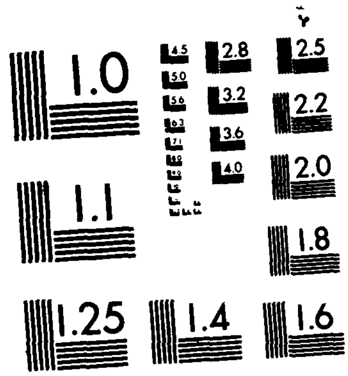

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THE IMPACT OF VHSIC TECHNOLOGY ON AUTOMATIC TEST SYSTEMS

Final Engineering Report

30 April 1987

Project Number 86-000-5

Item Number 0001, Sequence Number 1

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Author:

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FINAL REPORT

THE IMPACT OF VHSIC TECHNOLOGY ON AUTOMATIC TEST SYSTEMS

SOLICITATION NO. F33615-86-C-5079

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Prepared by:

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AIR FORCE BUSINESS RESEARCH MANAGEMENT CENTER/RDCB

AIR FORCE SYSTEMS COMMAND (AFSC)

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ABSTRACT

This effort defined the automatic testing requirement for VHSIC based system modules lending to the development of an Automatic Test System (ATS) architecture. The technologies needed to initiate the development of an ATS for VHSIC based systems and the characteristics of the expected population of VHSIC modules that will be developed over the next ten years were identified. Westinghouse interfaced with the various DoD agencies and contractors, including the VHSIC Phase II contractors, that have on-going efforts on VHSIC technology.

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LIST OF ACRONYMS AND ABBREVIATIONS

A/D	Analog/Digital
AF	Air Force
AFB	Air Force Base
AFBRMC	Air Force Business Research Management Center
AFHRL	Air Force Human Resources Laboratory
AFSC	Air Force Systems Command
AMTE	Automatic Microcircuit Test Equipment
ASA	Advanced Systems Architecture
ATE	Automatic Test Equipment
ATF	Advanced Tactical Fighter
ATS	Automatic Test System
BIT	Built-In-Test
BIU	Bus Interface Unit
CIIL	Control Interface Intermediate Language
CMOS	Complementary Metal Oxide Semiconductor
CND	Cannot Duplicate
CPU	Central Processing Unit
CSP	Common Signal Processor
D/A	Digital/Analog
DC	Direct Current
DRAM	Direct Random Access Memory

LIST OF ACRONYMS AND ABBREVIATIONS (cont'd)

E-O	Electro-Optical
ETM	Extended Test Maintenance
EW	Electronic Warfare
FD	Fault Detection
FFT	Fast Fourier Transform
FI	Fault Isolation
FOCUS	Data Base Name
GaAs	Gallium Arsenide
HSDB	High Speed Data Bus
IC	Integrated Circuit
I/O	Input/Output
ITA	Interface Test Adapter
LAN	Local Area Network
LRM	Line Replaceable Module
MADS	Maintenance and Diagnostic System
MASA	Modular Avionics System Architecture
MATE	Modular Automatic Test Equipment
MCI	Maintenance Control Interface
MHz	Megahertz
MIL-STD	Military Standard
MIPS	Million Instructions Per Second
MP	Maintenance Processor

LIST OF ACRONYMS AND ABBREVIATIONS (cont'd)

MMP	Module Maintenance Processor
MSI	Medium Scale Integrated Circuits
NMOS	N Metal Oxide Semiconductor
PDDV	Program Development and Device Verification
PI	Parallel Interface
PSP	Programmable Signal Processor
RAM	Random Access Memory
RETOK	Retest OK
ROM	Read Only Memory
SEM	Standardized Electronic Module
SIA	Switching Interface Assembly
SOS	Silicon-On-Sapphire
SRAM	Sequential Random Access Memory
TADE	Test And Diagnostic Equipment
TCA	Transmit Control Assemblies
TDA	Tests, Diagnostics and Analysis
TISSS	Tester Independent Software Support System
T/M	Test Maintenance
TMA	Test Module Adapter
TSMD	Time Stress Measurement Device

LIST OF ACRONYMS AND ABBREVIATIONS (cont'd)

TTL	Transistor-Transistor Logic
TVL	Test Vector Language
UDB	Unified Data Base
USAF	United States Air Force
UUT	Unit Under Test
VHDL	VHSIC Hardware Descriptive Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integrated Circuit
VTMA	VHSIC Test Module Adapter
WPAFB	Wright-Patterson Air Force Base

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ADVANCED DIAGNOSTICS TECHNOLOGY APPLICATION PROGRAM (ADTAP)

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The helpful cooperation of various DoD agencies and contractors that have on-going efforts on VHSIC technology were essential in the generation of the Westinghouse knowledge data base. The VHSIC ATS Survey Points of Contact that contributed data to this study are listed on the next page.

VHSIC ATS SURVEY POINTS OF CONTACT

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1.0 INTRODUCTION

The primary output of this study contract as defined by the sponsoring organization is to determine a generic VHSIC ATS architecture for VHSIC-based Line Replaceable Modules (LRMs). This was accomplished by a systematic evaluation of all known factors impacting architecture considerations. A recommended architecture was formulated by combining VHSIC-based LRM characteristics (technology implementation, performance parameters and imposed standards) with ATS requirements (technology/test methods and test equipment standards).

The VHSIC-based LRM survey, conducted as part of the contract workscope, has currently yielded data on a population of 29 LRM's. The survey information has been entered and compiled in the VHSIC ATS Knowledge Base. Querying the Knowledge Base using selected sort criteria (Appendix E) indicates a wide variety of implementations in both circuit complexity (MSI through VLSI) and processes (bipolar, CMOS, GaAs, etc.) to achieve LRM functions (VHSIC and non-VHSIC). The range of these implementations impose an equally wide range of requirements in the technologies used in the ATS if at-speed testing is to be realized. Additionally, an organic test program capability for the ATS will be required to resolve ambiguities at the chip level for fault isolation procedures.

The dominant force imposing architecture constraints on the development of VHSIC-based LRMs is the Pave Pillar/Pave Sprinter Advanced System Architectures (ASAs) programs. The goals of these demonstration programs are to have avionics technology development and compatible maintenance support in place for use in advanced fighter aircraft. A companion document to ASA is Air Force Regulation 800-45 Modular Avionics System Architecture (MASA). MASA establishes the maintenance concepts required to support an integrated avionics system.

Planned LRM standards from Pave Pillar, MASA, and MIL-STD documents are not uniformly applied to VHSIC-based LRM designs by the vendors. Both electrical and physical standards do not exist among different LRM vendors and in many cases among the same vendor's LRMs. This represents a serious threat to attaining a generic ATS architecture for VHSIC-based LRMs.

The TISSS interface to ATS is a fundamental requirement. The MASA driven TISSS/Unified Data Base (UDB) link will serve to link failure trend data, a rule base AI system to streamline test program selection, and the design engineer's VHSIC Hardware Descriptive Language (VHDL) simulation and timing analysis. Application specific test requirements are basic drivers of the ATS and are needed for test flexibility from the device to a module suite or LRU.

ATS standards for VHSIC-based LRMs are just beginning to evolve. The only VHSIC ATS standards that have been identified have been driven by the AF MASA document and Modular Automatic Test Equipment (MATE) VHSIC integration efforts. A possible method of linking existing MATE architecture to VHSIC LRM testing is discussed. In order to minimize life cycle costs (LCC) for the ATS to test existing as well as new and emerging technologies used in LRMs, a generic or open architecture will be required. Such a "technology transparent" ATS will necessitate the use of "smart" or managed interfaces between the ATS and LRMs. A top level functional diagram illustrating this architecture is shown in Figure 1-1.

Conclusions were drawn based on impacts associated with the implementation of a generic architecture versus a non-generic architecture. With the assumption that at speed testing will only be achieved with "VHSIC testing VHSIC", an open architecture which exploits managed bus interfaces will result in the lowest logistics impact and life cycle cost burdens. This approach is not hardware intensive and is compatible with existing Intermediate and depot ATE. An application specific (Active) interface test adapter will effect an economic and flexible VHSIC LRM tester. Depot involvement in advanced system SOWs must be expanded to preclude the proliferation of new test methodologies and support equipment.

It is recommended that a tri-service standards review committee be established. Their primary role would be to monitor conformance of prime mission equipment and support equipment to DoD VHSIC bus standards. To demonstrate the open architecture approach to ATE retrofit for VHSIC, an application specific interface test adapter should be developed. This demonstration should use fielded test equipment as a baseline for proof-of-concept. The standards review committee should monitor test and evaluation of technology transparent adapters and establish ATS drivers accordingly.

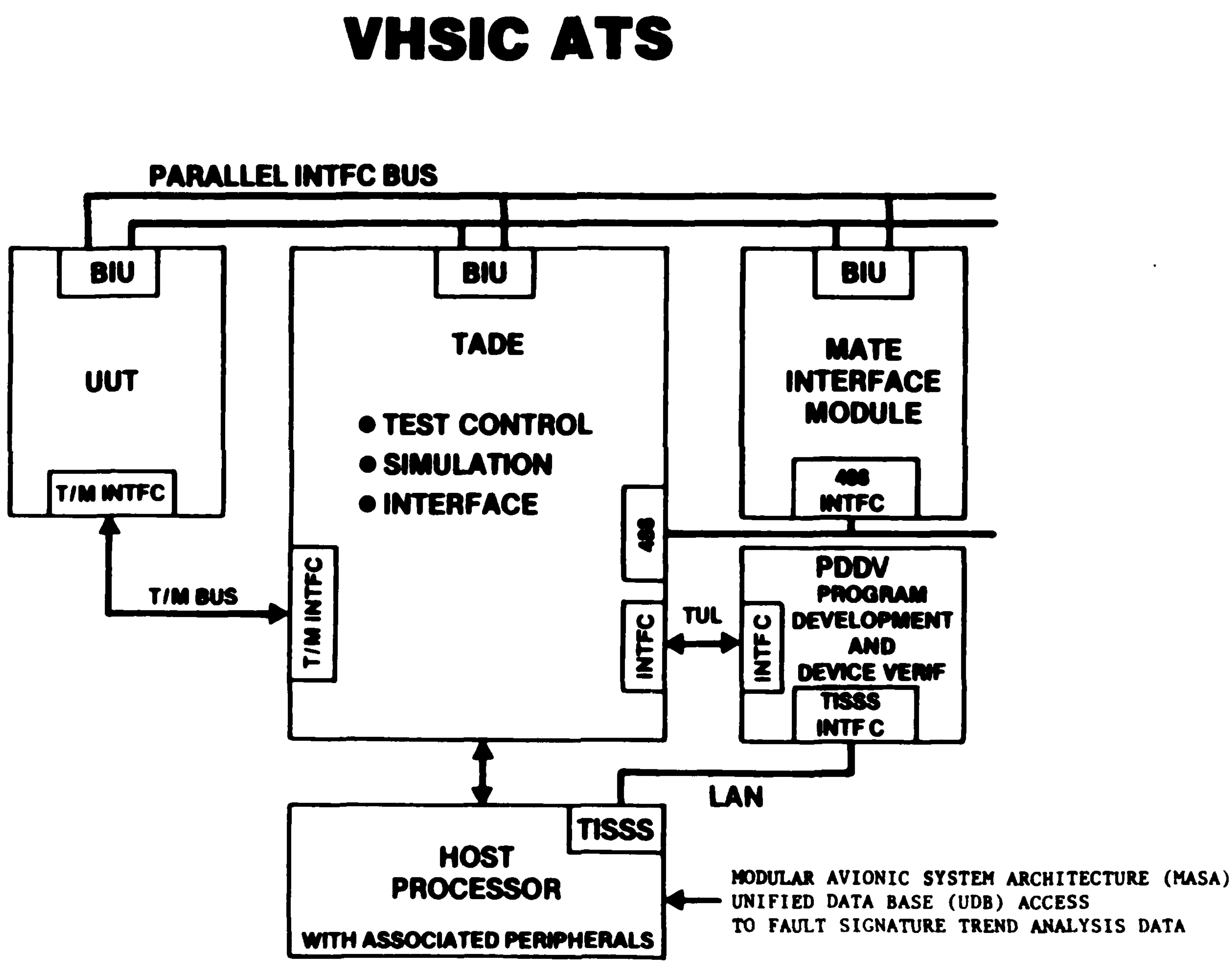


Figure 1-1. Generic VHSIC ATS Architecture

2.0 ATS ARCHITECTURE CONSIDERATIONS

The primary output of this study contract as defined by the sponsoring organization is to determine a generic VHSIC ATS architecture for VHSIC-based LRM's. The result was accomplished by a systematic evaluation of all known factors impacting architecture considerations including combining VHSIC-based LRM characteristics (technology implementation, performance parameters and imposed standards) with ATS requirements (technology/test methods and test equipment standards).

2.1 VHSIC-Based LRM Technology Impacts

The VHSIC-based LRM survey, conducted as part of the contract workscope, has currently yielded data on a population of 29 LRM's. The survey information has been entered and compiled in the VHSIC ATS Knowledge Base which Westinghouse will deliver at the conclusion of this contract.

A total of sixteen (16) data base sorts were run under the FOCUS Operating System control to extract data trends necessary to evaluate architecture impacts. Four (4) data base sorts (11 through 13A) were run to examine the LRM implementation technologies. The data sorts are detailed in Appendix E and are accompanied by summary observations.

The technologies were first sorted by VHSIC I and VHSIC II vs. module function (sorts 11 and 12). Eighteen (18) modules used VHSIC I chips for technology implementation and seven (7) modules used VHSIC II chips for this purpose. The VHSIC processes used to fabricate these chips included bipolar, NMOS and CMOS. A CMOS/SOS process was not included in these sorts since the VHSIC contractor (Hughes) that used this process to fabricate its VHSIC I chips did not contribute to the LRM survey. Process identification is needed to aid the design of process integrity test methods for the ATS. Examples of these tests are threshold tests for leakage current and logic levels.

Two additional sorts by module function (13 and 13A) were run to review technologies other than VHSIC that were employed in LRM implementation. The sorts produced a range of custom, semicustom, and gate array devices with MSI through VLSI complexities. Device functions included logic arrays, CPU's, array processors, arithmetic units, buffers and drivers, and a host of memory functions (RAMS, ROMS, DRAMS, and SRAMS). Linear circuits operating in an E-O environment were included in a Honeywell E-O signal processor. In addition, this module included a device type fabricated with a GaAs process. No functional description of this device was provided but it is assumed to be a digital device with VHSIC-like data rates.

In general, operating parameter information was not provided or limited only to signal processor performance specifications. The maximum operating rate was quoted as 3-5 MIPS (million instructions per second) for a VHSIC 1750A signal processor to be used as an LRM insertion into the F-15 central computer. However, since both VHSIC I and II are employed in the modules, maximum clock and data rate performance, consistent with VHSIC capability, can be expected. These rates currently are listed as:

	Max Clock Rate (MHz)	Max Data Rate (MHz)
VHSIC I	50	25
VHSIC II	100	50

Among the modules identified in the survey, VHSIC 1750A processor modules were dominant. Other modules that appeared in multiplicity included timing and control, FFT, high speed communication, I/O and memory. Interface and simulation of these module functions will be a prime responsibility of the VHSIC ATS during depot test and diagnostic procedures.

ATS LRM Technology Impact Summary

The requirements placed on the VHSIC ATS due to the technologies used to implement the LRM functions are many and varied. These technologies include both digital and analog circuitry. This will require A/D and D/A conversions for certain stimulus and measurement test and diagnostic routines. There is a broad range of circuit complexity (MSI through VLSI) in a mixture of processes: bipolar (TTL, VHSIC, and Linear), CMOS (VHSIC and non-VHSIC), NMOS (VHSIC and non-VHSIC), ECL, Linear (VHSIC), CMOS/SOS, GaAs, etc. In order to address these requirements in an at-speed testing environment, the ATS must have a large dynamic range of operation that extends from DC to 100 MHz.

ATS diagnostic and fault isolation procedures are compounded by the multiplicity of module functional types and circuit complexities. The ATS must have an organic test program development capability to resolve diagnostic ambiguities that will occur during chip fault isolation procedures. In these cases, the diagnostics supplied with the LRM will be supplemented by ATS generated test and diagnostic programs.

Circuit complexity presents additional challenges to the VHSIC ATS. In particular, densely configured VLSI/VHSIC circuits with embedded memory restrict access to ATS functional verification tests. If these circuits cannot be verified through control of built-in-test (BIT) circuitry, the ATS must be able to isolate a faulty component using application-specific tests hierarchically applied. This will require an avionics simulation capability within the ATS that conditions the LRM to the system operational mode at time of failure to allow fault ambiguity resolution. Additional fault detection (FD)/fault isolation (FI) assistance for the ATS may be realized through the use of redundancy and/or reconfigurability characteristics of both the VHSIC LRM's and chips. Using these features to configure the suspect component the same as a known good component will allow comparison tests to be conducted that will enhance FD/FI procedures.

The VHSIC LRM survey data does not show a reconfigurable component capability from any of the responding vendors. However, VHSIC technology will provide this capability and the architecture of the ATS should be planned to take advantage of this VHSIC feature to aid FD/FI procedures.

2.2 VHSIC-Based LRM Imposed Standards

The dominant force imposing architecture constraints on the development of VHSIC-based LRM's is the Pave Pillar/Pave Sprinter Advanced System Architectures (ASA's) programs. The goals of these modular avionics demonstration programs are to have avionics technology development and compatible maintenance support in place for use in advanced fighter aircraft starting with the ATF.

A companion document to ASA is Air Force Regulation 800-45 Modular Avionics Architecture (MASA). MASA establishes the maintenance concepts required to support an integrated avionics system. A concise summary of MASA regulations and linkage to LRM avionics system architecture is presented in Appendix D. This document describes on-line/off-line operation of the Aircraft MASA Suite and on-equipment/off-equipment LRM maintenance procedures. This description was used in conjunction with the vendor LRM survey data to determine additional ATS architecture considerations.

Significant requirements placed on VHSIC-based LRM's by the MASA document include autonomous maintenance capability; FD/FI for faults affecting system performance (96%/98% respectively) on LRM recording of fault history and Time Stress Measurement Data (TSMD); standard maintenance bus for test and maintenance (T/M) data; interoperability between LRM's and chips within an LRM; and a LRM maintenance processor (MP) for T/M data transfer, test, and configuration control. A number of sorts were run on the ATS knowledge base to examine the degree of LRM design conformance to these and other standards.

The data sort details and summary observations are shown in Appendix E. Sort 1 examined the availability of an on-module BIT processor (MP) that would provide an autonomous test processor capability and module chip set testability schemes. Sixty-two percent of the modules did not use on-board maintenance processors. Testability schemes for module VHSIC/VLSI devices showed a predominance of serial scan techniques; both boundary scan and set scan. These were generally used in conjunction with signature analysis self test to provide total device testability. Significant use of on-chip test vector generation using psuedo-random test pattern generation from seed vectors was also apparent.

Sorts 2 and 2A were run to provide additional information about the on-board maintenance processors (MP) identified in sort 1. Typical details provided by sort 2 for the MP's included operating system emphasized, provisions for fault history storage and maintenance bus description. The majority of these details were dedicated to a 4-wire maintenance T/M bus. Several listings included use of the 1750A instruction set in an Ada environment. On-board fault history storage was listed in two replies. The I/O terminator module from TI listed the most features on its MP (Ada, IEEE-488 bus, ETM and T/M bus operation).

Sort 2A lists LRM maintenance bus interface description information in addition to the MP bus information in sort 2. This sort shows that every module in the sort contains a test/maintenance (T/M) bus. A total of 28 modules were listed in this sort and 11 of those listed included the extended test/maintenance (ETM) bus as an LRM bus interface. Texas Instruments and Westinghouse accounted for nine of these 11 ETM bus listings. The next sort (3) examines whether the maintenance buses listed in sorts 2 and 2A comply with Pave Pillar interoperability standards.

The Pave Pillar standard buses are the parallel interface (PI) bus used for inter-LRM control and data tasks; the test and maintenance (T/M) bus used for LRM maintenance operations and data transfer; the high speed data bus (HSDB), a fiber-optic bus used to transfer voluminous data between VHSIC subsystems; and the extended test maintenance (ETM) bus used to detect and isolate faults at the chip level within an LRM. A total of 17 of the 26 modules listed in sort 3 show fully Pave Pillar compliant PI and T/M busses. Only eight (8) of the modules listed a compliant ETM bus and TI modules accounted for five (5) of these listings. The HSDB was listed as being provided on seven (7) LRM's but two of these listing were not Pave Pillar compliant.

Additional sorts were prepared to examine LRM conformity for on-module TSMD's and physical standard electronic module (SEM) sizes. MASA calls for standard SEM E modules as the basic LRM functional building block of VHSIC systems. The concept is to functionally partition the VHSIC system using identical physical SEM E size elements with each LRM performing a complete function. Knowledge base sorts 4, 4A, and 5 were run to evaluate the survey LRM population conformance in these areas.

Sort 5 examines the on-module use of time stress measurement devices (TSMD's) in conjunction with an autonomous module maintenance processor. None of the 28 LRM's in this sort show use of TSMD's. This means that on-LRM records of environmental overstresses will not be available to aid depot resolution of RETOK's and CND's.

Sorts 4 and 4A catalog the adherence of LRM physical dimensions to SEM military standard 1389. Data from both these sorts show that most vendors advertise SEM E compatibility but examination of their LRM physical dimensions show a wide difference in "standard" dimensions among vendors. There clearly is no agreement among vendors but this can be traced to interpretation of MIL-STD-1389. This standard, as presently constituted, is easily misinterpreted. Depot test fixturing will be greatly complicated unless this MIL-STD is clarified and attains compliance among VHSIC LRM vendors.

Sorts 6 and 7 summarize trends for mounting packaged devices to the LRMs and chips within these packages. Leaded surface mount and leadless chip carrier (LCC) LRM mounting techniques were prevalent among all vendors. Chip mounting in packages is diverse with different types of multichip packages, flat packages and dual-in-line packages being common choices. Depot component replacement techniques should be normalized around replacing complete packaged devices and ignore repairing multichip packages.

The knowledge base data sorts remaining to be discussed are sorts 8 through 10. Sorts 8 and 9 deal with LRM technology classification and functional characteristics. These issues were discussed in detail in the preceeding section (2.1). Sort 10 deals with LRM input power requirements and power dissipation. Input voltage requirements from all respondents show consistency and reflect 5V TTL, 3.3V VHSIC and 2V ECL logic levels. Power dissipation varies widely depending on module function and process technology with a range between 1.6 and 300 watts. Conduction cooling techniques defined for SEM modules will be severely taxed by some of these power dissipation levels.

Summary of LRM Imposed Standards

It is evident from the preceeding discussion that planned LRM standards from Pave Pillar, MASA, and MIL-STD documents are not uniformly applied to VHSIC-based LRM designs by the vendors. Both electrical and physical standards do not exist between different LRM vendors and in many cases among the same vendors' LRMs. This represents a serious threat to attaining a generic ATS architecture for VHSIC-based LRMs. However, most LRM's contain a Pave Pillar compliant PI bus and T/M bus. This will allow maintenance access by the ATS through compatible interface adapters. In this manner proper interface management by the ATS will allow a generic test and diagnostic interface. Physical differences in LRM configuration will jeopardize this "managed interface" concept since test fixturing variations may become unmanageable.

Due to the absence of a standard chip test bus (ETM), isolation to a faulty component will be immensely complicated. In addition, spare parts inventory will be adversely affected since there will be no interoperability at the chip level and parts substitution for failed chips will not be possible. This extends a severe burden on the depot repair facility.

2.3 ATS Technology/Test Methods Requirements

The VHSIC/ATS survey indicates that most advanced module types incorporate technologies ranging from discrete analog devices to VHSIC. Literature search includes new technologies such as analog VLSI or AVLSI. An example of AVLSI is the Integrated Services Digital Network which is a mixed-signal device. Therefore, on-module testability and depot test systems must be flexible to accommodate a range and mixture of technologies. Clock frequencies of VHSIC based systems will have to be emulated in ATS in addition to traditional parametric tests. ATS interfaces will access 25 to 50 MHz buses and high speed optical buses. ATS interface assemblies will require the same technologies as the Unit-Under-Test to accomplish true functional testing.

In anticipation of chip densities outlined in appendix C of this study, the DoD has directed that VHSIC chips contain their own on-device stimulus and measurement capability. In addition, VHSIC chips must have dedicated communications to the next higher level of test to report internal faults. Hierarchical test is a critical driver in the DoD VHSIC Program Office and in the MASA Air Force Regulation 800-45 which is outlined in appendix D.

The VHSIC/ATS Knowledge base yielded LRM testability considerations by each vendor. Of the sixteen sorts, sort 1 was assembled to discern vendor commitment to hierarchical testing utilizing an on-board maintenance processor and to determine LRM testability schemes. On-line or non-intrusive techniques were evaluated in addition to off-line or intrusive test approaches (refer to Appendix B). It was apparent that module function and complexity was proportional to built in self test (BIST) capabilities. Module types such as the Honeywell High Speed Electro-optical Signal Processor and the Westinghouse VHSIC 1750A employed on-board test controllers. Less dense board types such as IBM I/O and PI-bus terminators employed no BIST.

Of the vendors surveyed and from VHSIC specification literature, bus orientation towards phase 2 standards such as the Parallel Interface (PI) bus, the Test/Maintenance (T/M) bus, and the Extended Test/Maintenance (ETM) bus was limited. Tacit acceptance of these buses is apparent from questionnaire follow-up discussions. Sort 2A (refer to Appendix E) indicates that, of the vendors surveyed, all are including LRM access via the Test/Maintenance Bus. According to this sort, phase 1 VHSIC users are including the inter-chip Extended Test/Maintenance Bus. Follow-up discussions with several vendors indicated that modified or limited versions of the ETM Bus were going to be implemented (note: the ETM Bus Specification, version 1.1,is under promulgation as of this writing). Performance characteristics of the ETM Bus include: a 6.25 MHz clock; unidirectional data lines; 7 pin bus signals in ring or star configuration; and, TTL compatible loading. The Test Maintenance Bus is a 12 MHz serial bus consisting of a clock, two data lines, and a control line. Automatic Test Systems will have to be compatible with the T/M bus for module types utilizing an on-board maintenance processor. ATS will require bus compatibility with the ETM Bus for modules without a maintenance processor and for fault isolation to a faulty chip. Where these standard buses are not implemented or where hybrid configurations of these buses are used, ATS will require peculiar test interface units (TIUs) with unique software interpreters for VLSI/VHSIC.

In addition to the standard VHSIC buses, several vendors including IBM have established unique buses (refer to sort 3, Appendix E). Within the Common Signal Processor (CSP), IBM has incorporated an Element Control Bus, an Element Maintenance Bus, an ETM bus, a Parallel Interface (PI) Bus, a system breakpoint line, a system reset line, and a T/M Bus. These non-standard ,VHSIC buses will require at speed testing in addition to their use in parametric tests.

The Parallel Interface (PI) Bus is a standard bus utilized by all the vendors surveyed. The PI Bus which clocks 16 or 32 bit words at 25 MHz requires standardized Bus Interface Units (BIUs). BIUs designed to handle 25 MHz rates will be implemented in phase 2 VHSIC. As such, the ATS will have to have data rate flexibility and will have to interface with non-VHSIC, VHSIC phase 1, and VHSIC phase 2 BIUs.

The standard PI Bus, T/M Bus, and ETM Bus are directed by the MASA Air Force Regulation (refer to Appendix D). The MASA document indicates that "depot Automatic Test Equipment

(ATE) must test digital, analog, and RF/Microwave electronics. MASA ATE will interface with maintenance processors and controller for BIT; perform parameter value testing; perform functional logic testing; and dynamically test performance functions at clock speed under realistic signal environments." MASA indicates that Automatic Microcircuit Test Equipment (AMTE) shall be incorporated in ATE. However, chip parametric testing and characteristics will best be managed in a depot ATME incoming inspection and device characterization facility. The ATS will perform functional and at-speed verification testing of devices prior to insertion in the LRM under repair. This task will be the responsibility of the ATS chip verifier.

The Tester Independent Support Software System (TISSS - reference Appendix G) will serve as a link between the ATE or ATS and the AMTE. Identical functional level chip test programs will be shared by the AMTE and the ATS through the TISSS interface. MASA directs ATS standardization to accommodate test flexibility from the line replaceable unit (LRU) to the VHSIC device. This can only be achieved through standardization of avionic/ATS buses and exploitation of the TISSS interface.

The TISSS interface to ATS is a fundamental requirement. The MASA driven TISSS/Unified Data Base (UDB) link will serve to link failure trend data, a rule base AI system to streamline test program selection, and the design engineer's VHSIC Hardware Descriptive Language (VHDL) simulation and timing analysis. Anticipated in the depot maintenance scenario, is the fault isolation of several modules from one avionic suite. As such, the ATS will have to simulate aircraft interfaces. Short of using a "hot-mockup", the ATS will have to use multiple TISSS module/board descriptions to electrically simulate aircraft parameters. Basic aircraft parameters will include mission-specific functions, the High Speed Data Bus (HSDB) and the Mil-Std-1553B Bus. Environmental simulation of TSMD overstress conditions will also be required to resolve CND's and RETOK's. These application specific test requirements are basic drivers of the ATS and are needed for test flexibility from the device to a module suite or LRU.

In order to accomplish these diverse test and diagnostic procedures, the ATS must be implemented with technologies that are compatible with the population of LRM's being serviced. Portions of the ATS that will be speed and loading sensitive, will require utilization of VHSIC I & II technologies. RF VHSIC LRM's must also be considered as well as optical transmitters and receivers that connect to the ATF planned high speed fiber-optic link (HSDB). These LRM features will require special ATS interface designs and UUT test fixturing. This will probably mandate broader bandwidth devices than VHSIC. GaAs and hybrid optoelectronic devices will be candidates for these applications.

It should be emphasized that the ATS will be primarily a bus oriented system that must be self-sustaining in the diagnostic and test program development areas. It will interface naturally with the emerging VHSIC design and maintenance support structures for chips, LRM's, and systems. The most significant threat to ATS effectivity would be lack of interoperability at the LRM and chip levels. This would require a massive inventory overhead for special interfaces and diagnostic and fault isolation software. This result would preclude a generic ATS architecture approach. Every effort should be extended to effect interoperability for LRM's and systems in order to simplify depot tasks and prevent inordinate costly growth of VHSIC support facilities.

2.4 ATS Test Equipment Imposed Standards

ATS standards for VHSIC-based LRM's are just beginning to evolve. This is largely due to availability of LRM's to be tested. The universe of LRM's that was identified during this study contract, to a large extent, represent planned LRM developments. There is an on-going VHSIC insertion program sponsored by the Tri-Service VHSIC Program Office to demonstrate the benefits of VHSIC technology insertion into DoD weapons systems.

The first actual insertion involved replacing one of the Tranmit Control Assemblies (TCA) in the ALQ-131 EW system with a hybrid assembly containing a combination of VHSIC and non-VHSIC chips. The stated goal of this insertion was to improve the operational availability of the ALQ-131 system. The improvement involved the application of VHSIC I chip technology into the digital TCA and restructuring of the architecture for testability. TRW was the VHSIC AF contractor for this program and their Maintenance and Diagnostic System (MADS) provided the self test capability that would allow fault isolation to the SRU level (Refer to Appendix B, TRW Approach). A brassboard model of this insertion was demonstrated in late 1986.

The information on this insertion and the AFWAL VHSIC 1750A module set was solicited from TRW by the VHSIC ATS Survey Team. However, TRW declined to supply the V1750A module set data due to competitive concerns and, while agreeing to supply ALQ-131 TCA insertion data, have not as yet responded.

The only VHSIC ATS standards that have been identified have been driven by the AF MASA document and Modular Automatic Test Equipment (MATE) VHSIC integration efforts. MASA specifies that depot ATE must comply with MASA technical requirements. These are summarized in Appendix D of this report. Additionally, MASA defines that the architectural and interface standards in MATE Development Guide 2 (28-00642 Rev. B) shall be used when these technologies can support the testing requirement. If these technologies are found inadequate, the vendor shall develop the capability required. The vendor shall prepare and submit a guide improvement form per Guide 0, that identifies changes required to the MATE guides to support the technology.

The rationale underlying the MASA and MATE VHSIC standardization efforts is to provide an effective integration of MATE and VHSIC technology. This task, while formidable, appears to be achievable. The major difficulty in this integration is to determine a compatible method of testing MATE and VHSIC modules in the same UUT.

A typical MATE configuration for depot support equipment is diagrammed in Figure 2-1. This illustrates the major components of the MATE architecture and how they interact with a LRM UUT. The test controller is a MIL-STD-1750A CPU using a JOVIAL operating software system. The test language is ATLAS and all test instruments are interfaced to an instrument standard IEEE-488 bus. The 1750A CPU selects the instruments needing to supply stimulus and response measurements to the UUT in accordance with the ATLAS test program. Stimulus and response signals are connected to the UUT through a switching interface assembly (SIA) and an

MAJOR COMPONENTS OF THE MATE SYSTEM FOR SE

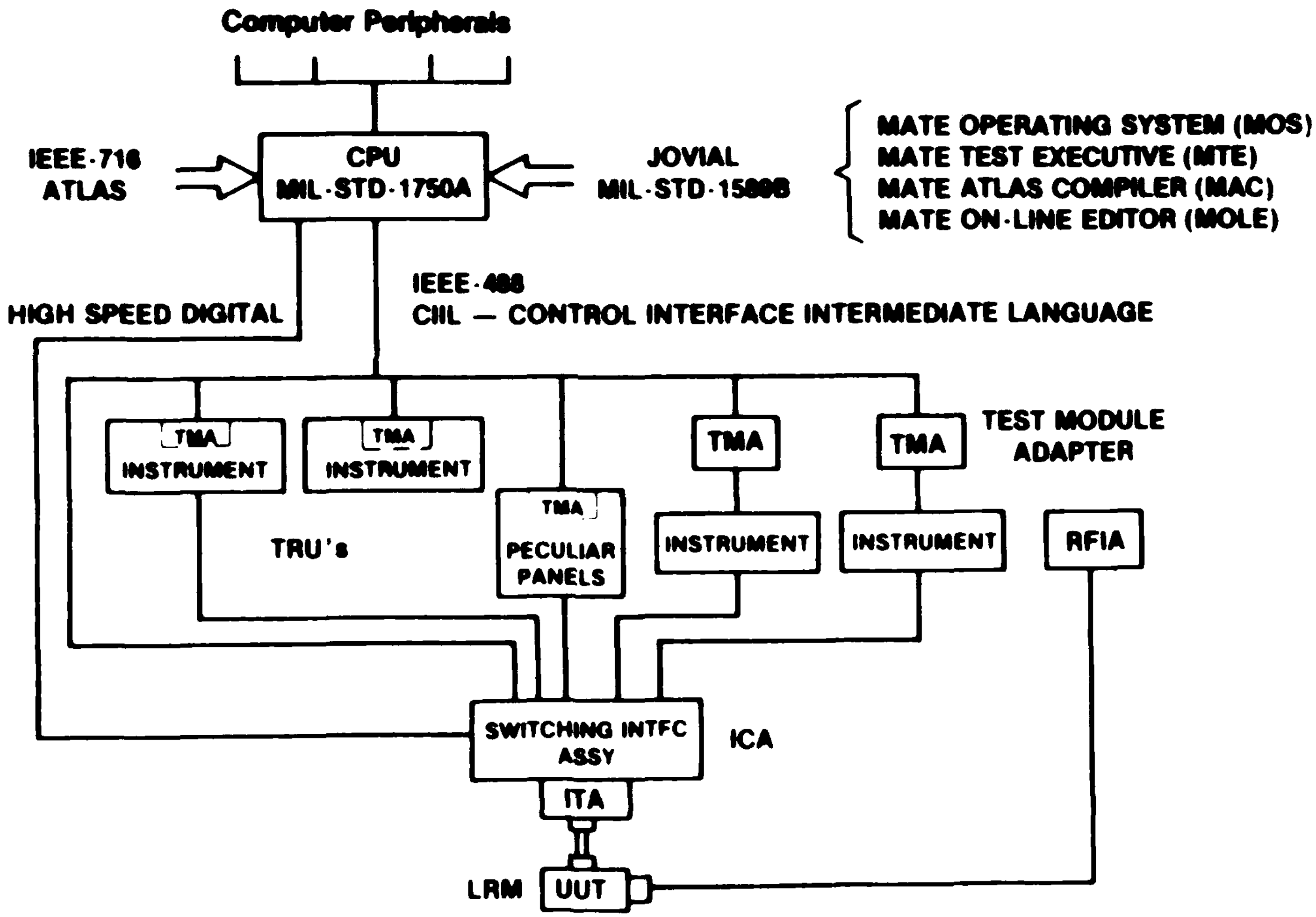


Figure 2-1

interface test adapter (ITA). Interoperability of test instruments and peculiar panels is accomplished by employing a common control language and standard bus communications protocol on the IEEE-488 bus. The common language is CIIL (Control Interface Intermediate Language). Individual instruments use a microprocessor controlled test module adapter (TMA) to provide a CIIL compatible communications interface with the bus. MASA specifies that, if possible, the MATE testing architecture be applied to testing VHSIC LRM's. If this is not achievable, then acceptable methods must be determined. A possible method of linking existing MATE architecture to VHSIC LRM testing is diagrammed in Figure 2-2. Examination of this diagram shows a UUT assembly composed of VHSIC LRM's interconnected to a MATE testing system previously described. The difference in test rates between VHSIC and current systems tested under MATE is the major incompatibility. The approach to resolving this condition is to incorporate a TMA VHSIC interface between the UUT VHSIC control bus and the IEEE-488 bus. This interface is illustrated in the diagram.

The VHSIC TMA contains an IEEE-488 interface that communicates with the MATE controller in CIIL. In addition, the VHSIC TMA (VTMA) contains a high speed local memory that is connected between the 488 IC and a resident VHSIC CPU that is tied to the VHSIC control bus. Test vectors for the VHSIC LRM's can be loaded into the VTMA high speed memory at the relatively slow IEEE-488 rate. Once RAM loading is complete the VHSIC CPU can apply these test vectors over the VHSIC control bus (PI bus) to the VHSIC LRM's connected to this bus. In this way, at-speed VHSIC test can be performed under control of the MATE test controller.

DEPOT MAINTENANCE VHSIC INSERTION MATE INTERFACE

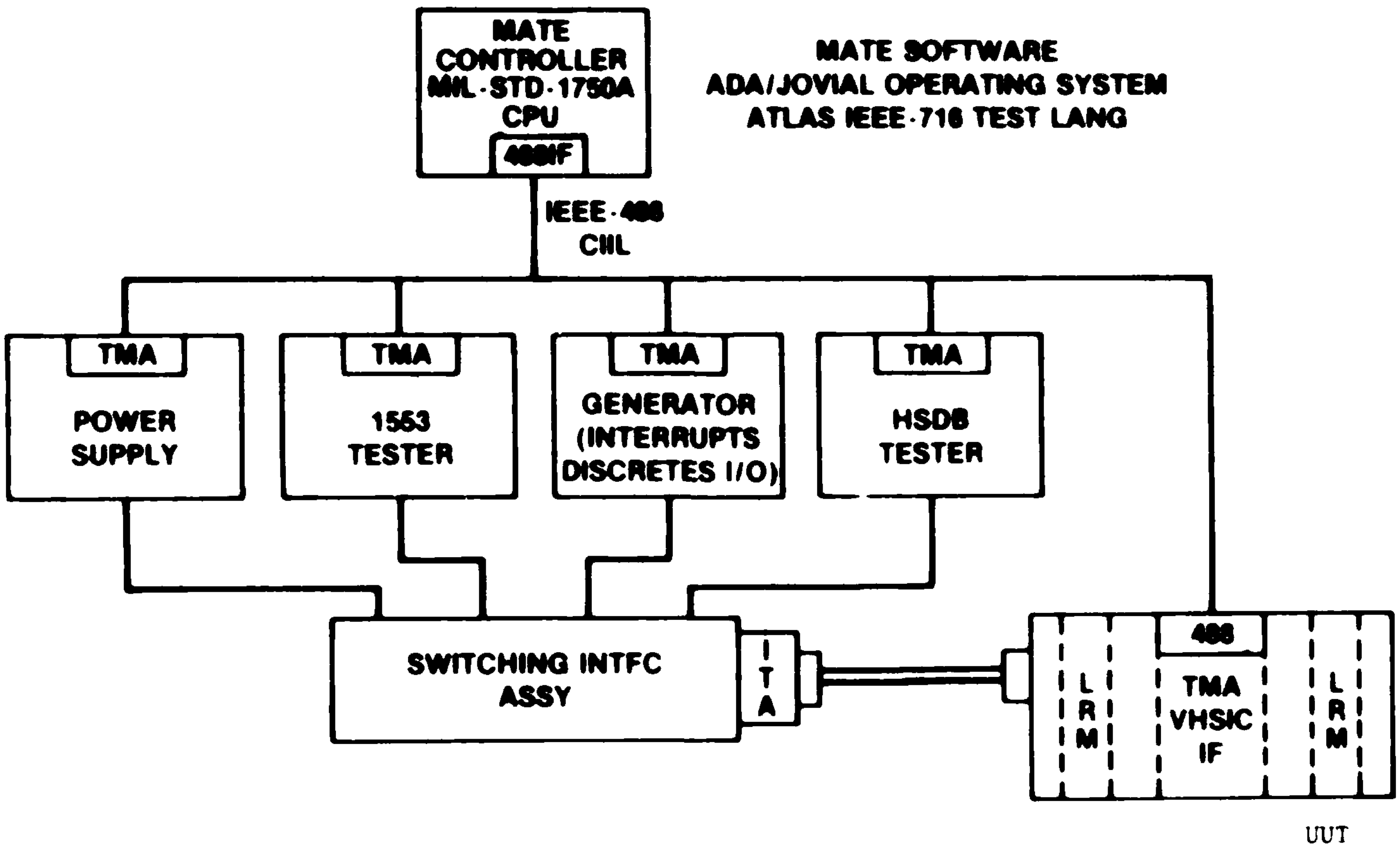


Figure 2-2

Any non-VHSIC modules within the UUT can still be accessed in the conventional manner through the SIA and ITA connections shown. Therefore, it appears to be possible to provide compatible testing of systems containing VHSIC and non-VHSIC LRM's with the existing MATE architecture.

2.5 Generic ATS Architecture and Discussion

The preceding sections used the study generated survey data to define the characteristics of the VHSIC based LRM's that influence a baseline architecture for the VHSIC ATS. VHSIC LRM operational and functional characteristics and implementation technologies were cataloged and evaluated. The impact of imposed LRM standards, both existing and planned, were studied for their impact on ATS requirements. This set of LRM induced demands was used to establish the ATS test methodologies needed for their satisfaction. Implementation of these test methodologies define the technology structure of the ATS. Finally, the imposed VHSIC and non-VHSIC standards that interact with the ATS were defined and their impact examined.

Conformance to these considerations require that the VHSIC ATS be structured in an "open architecture" with "managed interfaces." The distinctive characteristic of an open architecture is its flexibility in adapting to a broad range of test applications with minimum impact on the baseline ATS design. This is made possible by utilizing active interface test adapters (ITA's) that are application specific. All generic VHSIC ATS interface test adapters will have a common set of elements. This means that only a portion of the ITA ATS architecture is in effect "open" to an expanding population of test applications. Another way of describing this desired feature of a generic ATS is "Technology Transparent."

The study team has addressed this architectural concept in a set of hierarchical functional diagrams. The top level functional diagram is shown in Figure 2-3. The core element is the test and diagnostic equipment (TADE) which performs the fundamental ATS functions (test control, simulation and interface). The ATS "managed interface" concept can be studied by inspection of this diagram. TADE controls all traffic in and out of the ATS through three primary interfaces.

1. VHSIC Parallel Interface Bus (PI)
2. VHSIC Serial Test and Maintenance Bus (T/M)
3. IEEE-488 Standard Instrument Bus

Proper utilization and management of these buses (interfaces) by the TADE will allow ATS access to both VHSIC and non-VHSIC LRM's in a compatible environment. Baselining this ATS task is the key element in establishing a generic architecture.

Figure 2-3 illustrates a VHSIC based LRM as the UUT which is accessed by the ATS through both the PI and TM bus interfaces. Non-VHSIC LRM's that do not operate with a VHSIC standard bus structure are controlled by the TADE with the aid of the MATE Interface Module using IEEE-488 compatible testing. Requirements for supplemental test programs are accomplished by the ATS Test Program Development and Device Verification (PDDV) subsystem. This subsystem uses the Tester Independent Software Support System (TISSS) resident on the depot host processor to generate supplemental programs and other software development tasks. This subsystem inter-

VHSIC ATS

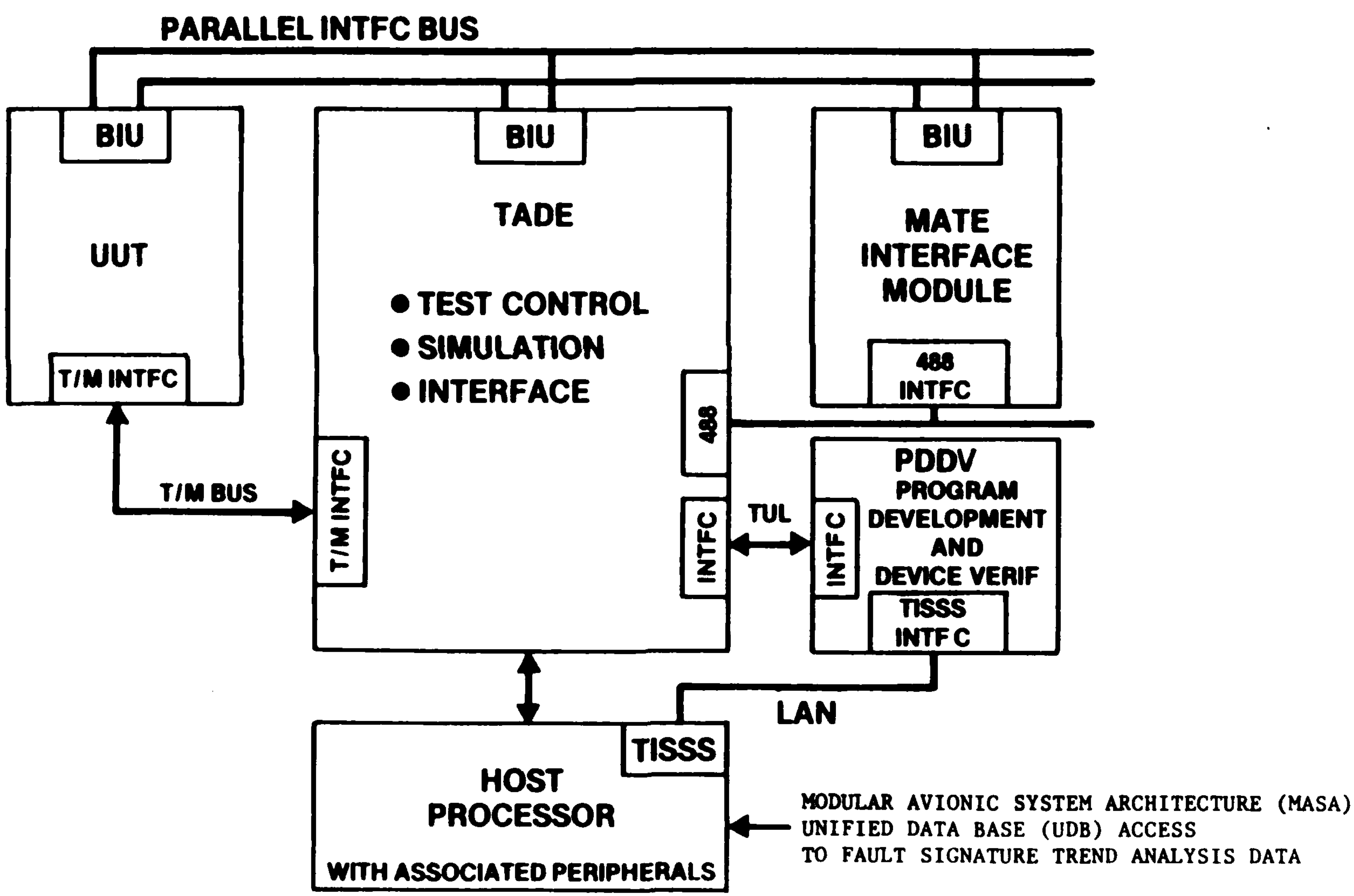


Figure 2-3

faces to the TADE via a test vector language (TVL) link. TVL is currently a language component of TISSS and is a subset of the VHSIC Hardware Descriptive Language (VHDL). A discussion of the TISSS is contained in Appendix G of this report.

An additional function of PDDV is verification of device components prior to insertion in LRM's being repaired. This device verification confirms device capability using a core set of verification tests that include:

1. initiation of bit testing via device maintenance node,
2. leakage and logic parametric tests to validate semiconductor process stability,
3. Application specific tests to validate at-speed performance.

Verification of devices prior to repair should be a depot requirement since the LRM chip remove and replace procedure for VHSIC/VLSI devices will not allow LRM repairs more than a few times at the same site. It should be noted that the VHSIC ATS device verifier does not perform a complete set of MIL-temperature range AC and DC parametric measurements. This exhaustive device testing would be accomplished on the depot AMTE which performs incoming inspection and characterization on VHSIC and non-VHSIC devices. The AMTE also utilizes the TISSS to generate device test programs from the device design data base.

The Depot Host Processor, in addition to the TISSS subsystem, also hosts the Unified Data Base (UDB). The UDB is tied into the base level data base through a data transfer link. MASA data is transferred to the UDB through a data path linking aircraft data from the MASA suite to the base level data base and through the data transfer link to the UDB. A complete MASA data flow diagram is shown in Appendix D. The UDB is used at the depot to evaluate fault signatures and LRM trend analysis.

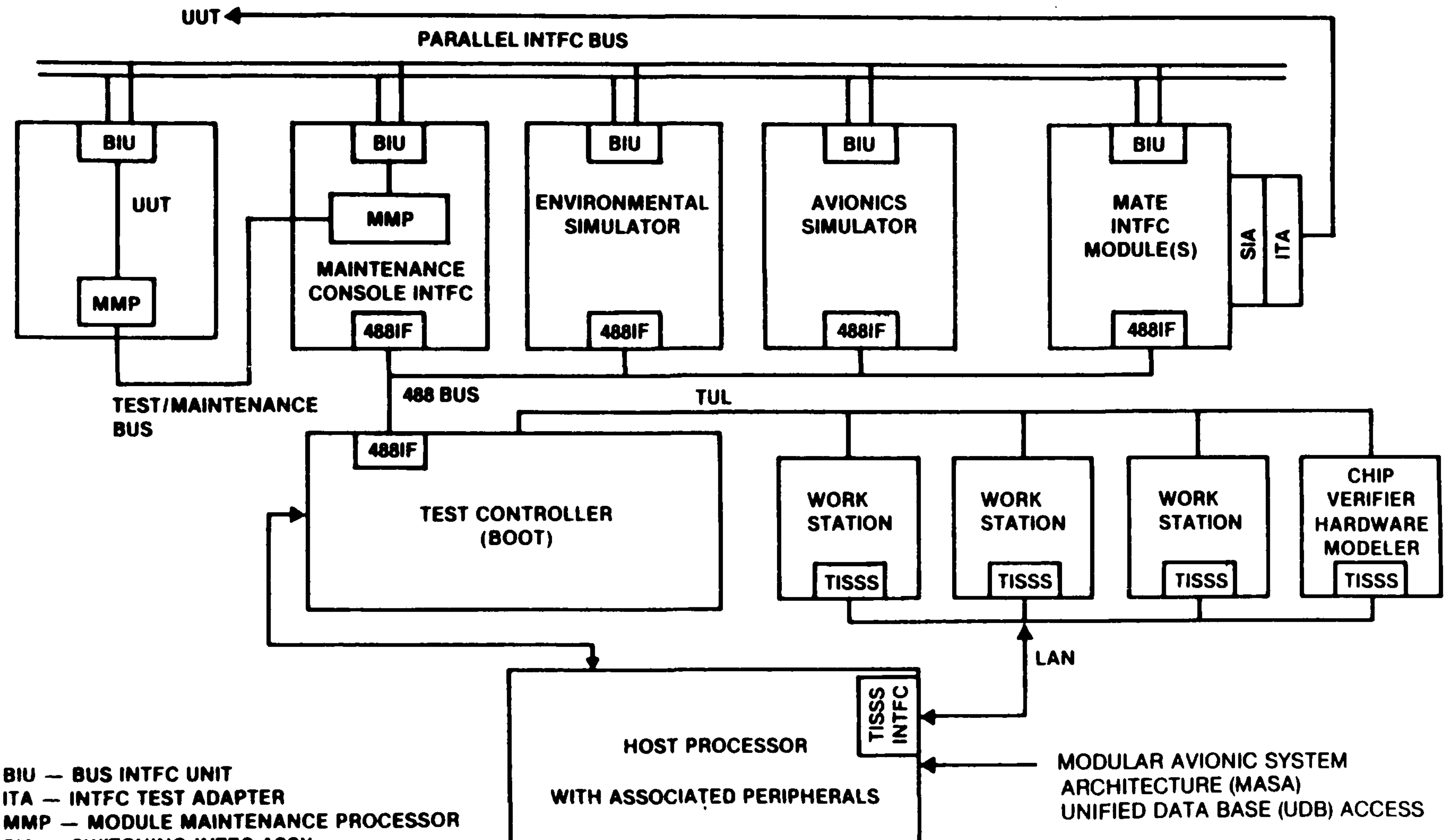
The architectural details of the TADE and PDDV will next be discussed. A second level ATS functional description outlining this information is diagrammed in Figure 2-4. This diagram shows the components of the TADE subsystem and are listed below.

1. Test Controller
2. Maintenance Console Interface
3. Environmental Simulator
4. Avionics Simulator

The test controller manages UUT test programs and diagnostic and fault isolation procedures. It interfaces to the UUT through the maintenance console interface (MCI). The MCI is an intelligent ITA and contains a resident VHSIC processor (MMP) that communicates with the UUT maintenance processor (MMP) via the T/M bus. A VHSIC standard bus interface unit (BIU) is used to connect both the MCI and the UUT to the PI bus. The UUT and the MCI have to be housed in the same test fixture since the maximum operating length of the PI bus for a data rate of 25 MHz is fourteen (14) inches. In fact, all modules shown in the diagram that connect to the PI bus would have to reside in the same physical container.

The other two TADE components (the environmental simulator and the avionics simulator) are provided to recreate the mission operational conditions that were present

VHSIC ATS



BIU — BUS INTFC UNIT
ITA — INTFC TEST ADAPTER
MMP — MODULE MAINTENANCE PROCESSOR
SIA — SWITCHING INTFC ASSY
TISSS — TESTER INDEPENDENT SOFTWARE SUPPORT SYSTEM
UUT — UNIT UNDER TEST

Figure 2-4

at the time of UUT failure. Their use precludes the need for providing an expensive "hot mockup" to simulate the external LRM interactions at the time of failure. They are managed by the test controller via the IEEE-488 bus.

The MATE interface module functions to interface additional stimulus and measurement instruments to a VHSIC UUT through the IEEE-488 access. In addition, it provides a connection to a complete MATE test of a non-VHSIC UUT through the switching interface adapter (SIA) and the interface test adapter (ITA).

The PDDV subsystem is comprised of a set of work-stations, a chip verifier and a hardware modeler. The components are clustered on a local area network (LAN) that provides TISSS access from the host processor. The PDDV components are also coupled to the test controller through the previously mentioned test vector language (TVL) link. This arrangement gives the PDDV the capability to use TISSS for test program development device simulation and design on the work stations. These tasks are complemented by the chip verifier which provides verfication of devices prior to repair insertion and modeling capability for devices without a design data base. The modeler also allows real time comparison between an actual device and a model generated on the workstation.

Much of the uniqueness of the ATS architecture is embodied in the MCI. Figure 2-5 shows both a functional and physical partitioning of this component. It provides external bus interfaces to the critical buses that the ATS must manage to qualify as a generic VHSIC LRM test system. The details are contained in Figure 2-6, the ATS MMP Functional Diagram.

MAINTENANCE CONSOLE INTERFACE

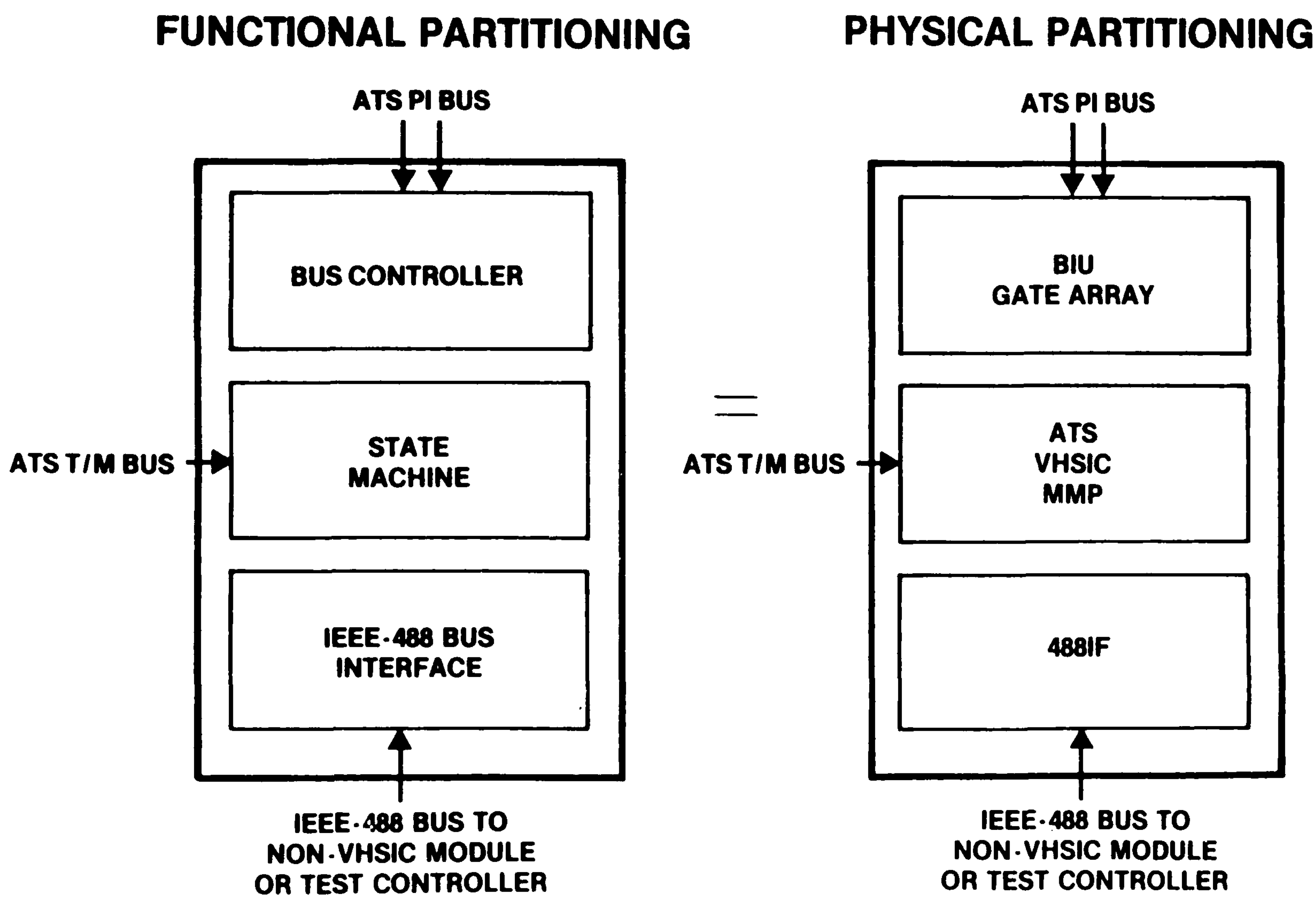


Figure 2-5

ATS MMP

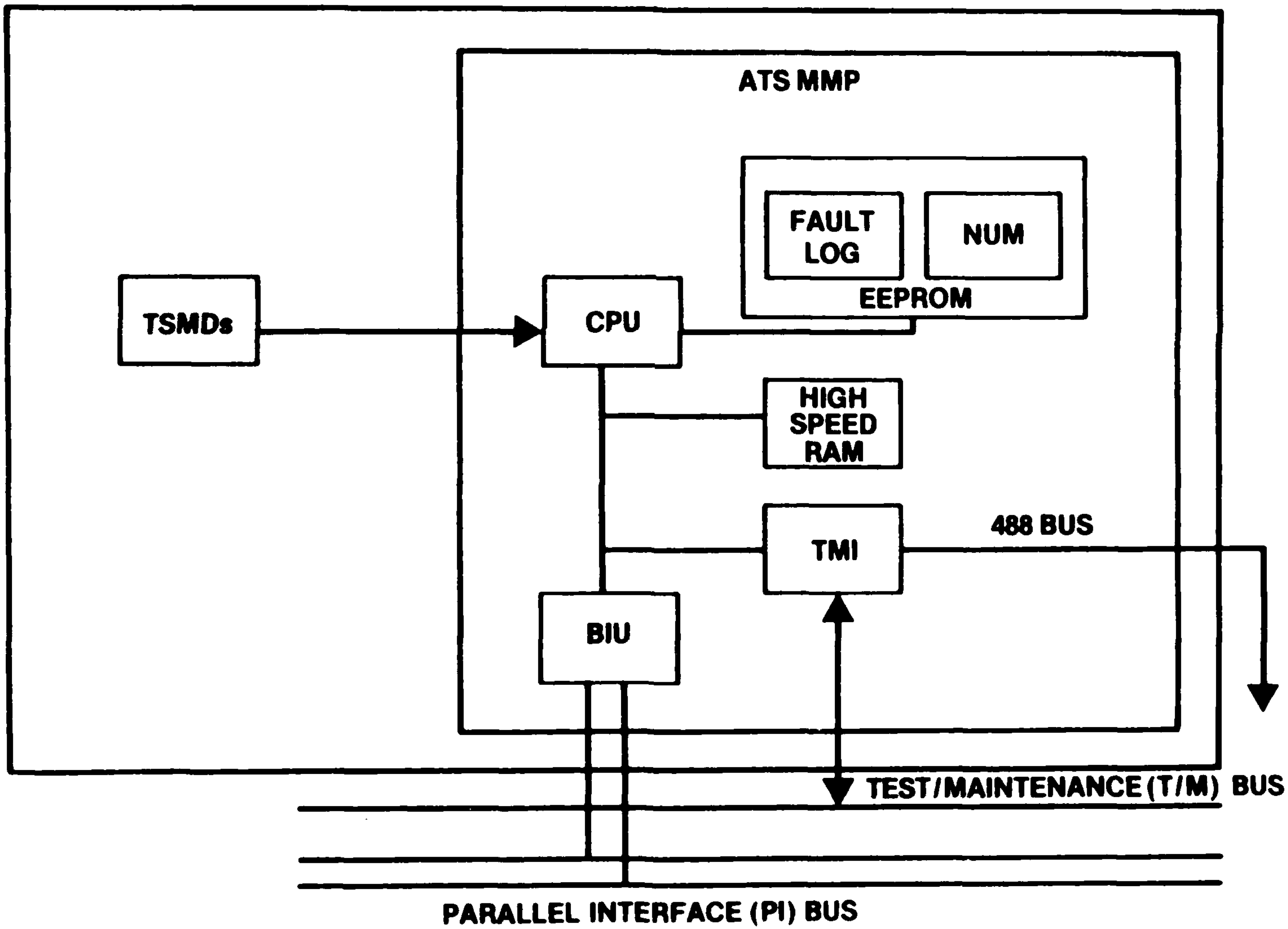


Figure 2-6

PI bus access is through the BIU to the VHSIC CPU which controls MMP self test and UUT fault test vector application. The EEPROM is a nonvolatile memory used for both UUT fault log and MMP program control. The test maintenance interface is used to condition signals and provide bus access to the high speed RAM and CPU from all three managed buses. A typical at-speed testing application would have the test controller load the high speed RAM with the required test vectors at IEEE-488 data rates. The CPU would then control application of these test vectors to the UUT using the path through the BIU and the PI bus. These tests could be applied at VHSIC rates since all components handling the test data would be VHSIC components. In this manner, the ATS would be using VHSIC to test VHSIC. Additional features of the ATS MMP are Time Stress Measurement Devices (TSMDs) which are used to compare outputs and calibrate the TSMD's resident in the LRM (MMP).

A functional diagram of a typical MMP architecture for a LRM is shown in Figure 2-7. This device provides a complete maintenance capability to the LRM (UUT) allowing autonomous LRM operation within a VHSIC system. The architecture is similar to the ATS MMP and it interfaces externally to both the PI and T/M bus. It provides a test maintenance interface TMI for VHSIC and non-VHSIC devices, both digital and analog. It accesses LRM functional circuitry through the extended test and maintenance (ETM) bus. The MMP controls logging of operational faults and environmental overstress during and between missions utilizing TSMD's. The MMP communicates with the ATS through T/M and PI bus operation.

In addition, the MMP has capability to reconfigure around degraded LRM circuitry to maintain full mission function. When the mission is completed, the remaining LRM

LRM MMP

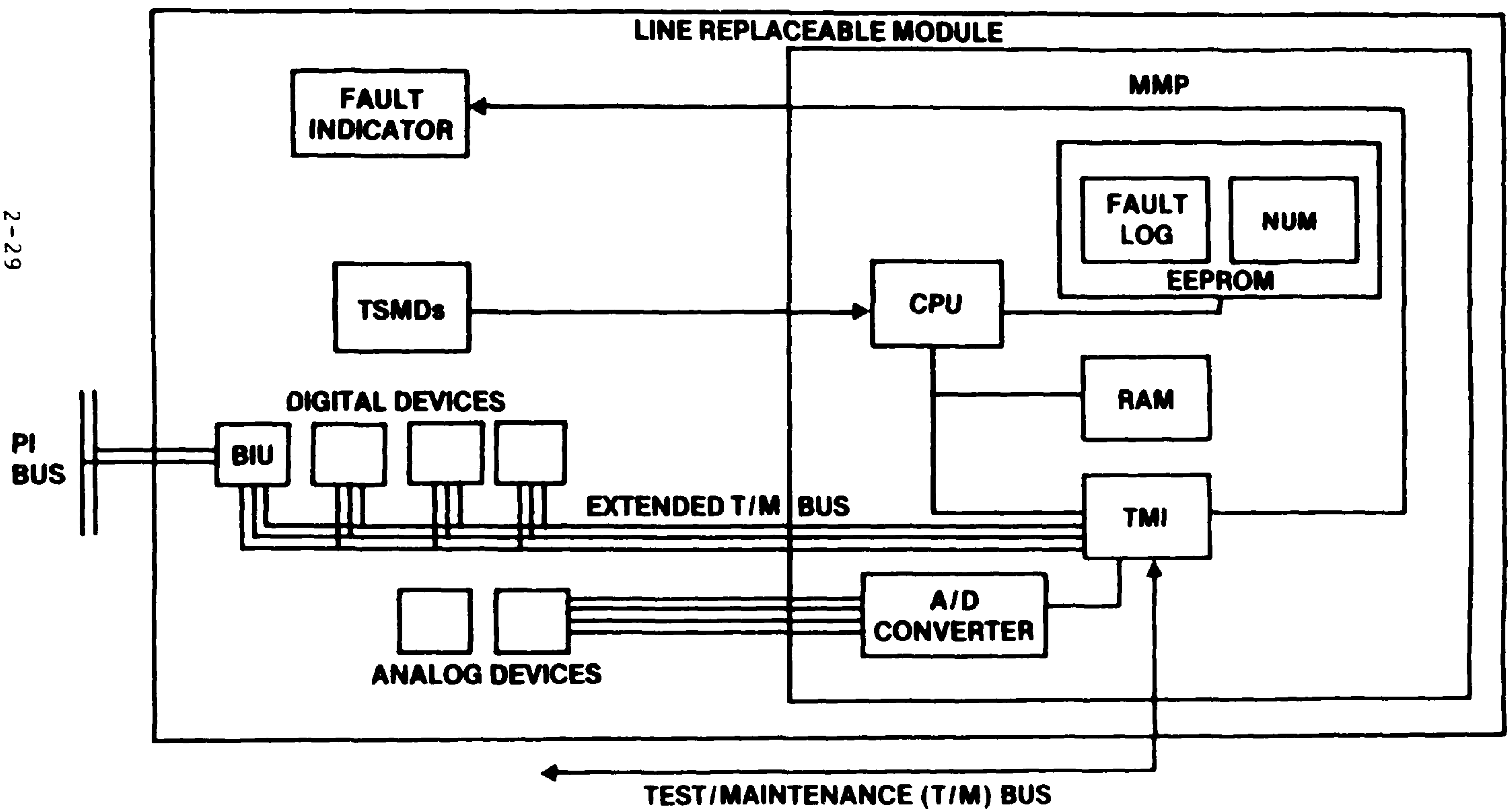


Figure 2-7

capability can be assessed during flight-line maintenance operations and a decision can be reached whether or not to return the LRM to the depot for repair. Assessment of repair or reconfiguration will also be a function of the depot VHSIC ATS when the LRM is returned for servicing. However, this function would normally be performed by the LRM configuration facility.

3.0 DEPOT IMPACTS

This study has focused on the realization of a viable economic architecture for a VHSIC-based LRM Automatic Test System (ATS). The preferred solution, a generic architecture was detailed in Section 2.5 of this report. The advantages and inherent risks involved in attaining a generic architecture will now be identified. They will be contrasted with the Depot consequences of a non-generic architecture to provide a basis for risk/benefit analysis of VHSIC ATS architectures.

3.1 Generic ATS Architecture

The dominant advantage of a generic ATS architecture is the ability to achieve a technology-transparent Depot ATS. This means that VHSIC and non-VHSIC LRM's can be serviced with the same ATS. (The open architecture and managed interface concept described in this report provides the technology-transparent solution.) The ATS is a bus-oriented test system utilizing "smart" technology. Specifically, interfaces to provide a controlled access path from the UUT to the appropriate ATS bus. This implementation insures adaptation of ATS architecture to new technologies ("open" architecture) while maintaining ATS bus control ("managed" interfaces).

This approach is not hardware intensive and is compatible with a wide range of test controllers that function with a standard IEEE-488 interface. The intelligent interface is an application-specific ITA which, due to test fixturing constraints, is colocated with the UUT. This configuration provides an effective economic support solution that is simple and flexible.

There are risks associated with achieving a generic ATS architecture solution. In particular, for VHSIC modules, the autonomous nature of LRM's, as defined by MASA, must exist. Equally important, VHSIC interoperability at the LRM and chip levels with appropriate standard bus structures described in this report must be maintained. These mandate continued coordination of VHSIC and non-VHSIC LRM and ATS standards by both weapons systems and support communities. The concepts must apply equally to VHSIC systems (insertions and new systems) and non-VHSIC systems (old and new technologies).

3.2 Non-Generic ATS Architecture

Failure to achieve a generic ATS architecture will place significant operational and economical burdens on the depot support structure. Specialized support will be required for VHSIC and non-VHSIC LRM's. New technology applications will require specific ATS architecture solutions that will preclude design interchangeability.

This lack of commonality among ATS interfaces will escalate software support and hardware fixturing costs. Documentation levels will be inordinately expanded and cumbersome to manage. In particular, fault isolation to the failed LRM component will be highly complicated, especially if a standard chip test bus (like the ETM bus) is nonexistent. Non-standard chip test bus access will preclude interoperability and interchangeability for VHSIC chips. This will severely burden LRM fault isolation repair procedures and spares inventory management. The result will be a high cost ATS solution with reduced effectiveness.

The inclusion of testability features (using PI and T/M busses) into VHSIC LRMs will keep the flight line maintenance philosophy workable. However, at the depot maintenance level, fault isolation and repair of LRMs will be severely curtailed with a non-generic ATS architecture. In particular, the unavailability of a standard chip test bus will result in a proliferation of unique support equipment types and their inherent costs.

4.0 CONCLUSIONS

The impacts of section 3.0 indicate the following conclusions:

- o New and emerging technologies could instigate a proliferation of new test methodologies, test equipment, and test support equipment unless managed across all programs. Depot involvement in advanced system SOWs should be expanded beyond support equipment to include Prime Mission Equipment (PME) design drivers which impact a Generic ATS.

- o A tri-Service standards review committee for VHSIC technology should be established to monitor conformance of systems and support equipment to critical standards and specifications.

- o Depot involvement in defining PME and ATS module maintenance controller architecture is paramount to achieving reduction of unique test equipment at the depot. Standards to manage module fault log data and time stress measurement device (TSMD) outputs are critical to depot large scale trend analysis.

- o Application-specific ATS interface test adapters associated with a generic ATS will minimize logistics and life cycle cost burdens for new technology weapons systems applications.

- o Chip level interoperability and interchangeability standards for test bus access must be employed. Functional interoperability through standard interfaces will reduce test program management and

ATS hardware modifications. Interchangeability is a critical depot need to preclude single source vendors. Single source chip supplies translate into parts procurement problems and LRM redesigns.

This report section will be completed/refined following AF sponsoring agency comments on report sections 2.0 (ATS Architecture Considerations) and 7.0 (Appendices).

5.0 Recommendations

- Generic ATS interface test adapters should be developed which minimize burdens associated with logistics and life cycle cost as new technologies are introduced. Specific depot and AIS test equipment should be selected to become baseline systems for VHSIC testability upgrades using the ATS architecture defined in figure 2-4. A proof-of-concept would serve to promote standardization at the PME and ATE level. VHSIC insertion in the F/FB-111 through the Pave Sprinter initiatives is feasible for demonstration. A technology specific (VHSIC) active interface test adapter for fielded ATE should be developed to prove that cost and logistics impacts to fielded intermediate and depot test equipment will be manageable.

- Standards to manage module fault log data and time stress measurement device (TSMD) outputs should be established in conjunction with emerging Air Force Programs such as the Integrated Maintenance and Information System (IMIS). The depot should develop a unified data base with which to exploit "failure mode signature" data to perform trend analysis. This will serve to reduce fault isolation and repair times in addition to establishing scheduled or prognostic maintenance for LRMs based on statistical analysis.

- A tri-Service group, under DoD leadership, should be established to develop and promulgate the Military Standards needed for the application and support of VHSIC. Proposed or existing standards which are subject to interpretation should be tightened to preclude ambiguity. Presently, ambiguities exist in Standard Electronic Module (SEM) and VHSIC bus standards. The Standards should be transparent to phase I and II VHSIC for implementation of chip (ETM) buses, module maintenance controllers, and LRM level buses.

- Chip level interoperability and interchangeabilty should be assessed under direction from a tri-Service committee to ensure minimal technical and logistics impacts. Applicable DoD level standards should follow in a timely manner prior to commencement of Advanced Tactical Fighter FSD.

6.0 REFERENCES

This report section will be completed following AF Sponsoring Agency comments on report sections 2.0 (ATS Architecture) and 7.0 (Appendices).

7.0 APPENDICES

APPENDIX A

EXISTING
STANDARDS EVALUATED FOR VHSIC/ATS
APPLICABILITY

Existing Standards

MIL-SPECS

MIL-E-5400	Electronic Equipment, Aerospace, General Spec for This specification covers the general requirements for airborne electronic equipment for operation primarily in piloted aircraft, missiles, boosters and allied vehicles.
MIL-S-19500	Semiconductor Devices, General Spec for This specification establishes the general requirements for semiconductor devices. Detail requirements and characteristics are specified in the detail specifications. Four levels of product assurance requirements are provided; differentiated by the prefixes: JAN, JANTX, JANTXV AND JANS. This specification provides for certification

of conformance and procurement traceability by the manufacturers who offer products described therein.

MIL-C-28754	Connectors, Electrical, Modular, and Component Parts, General Spec for This specification covers the general requirements for rack and panel connectors, base plate connectors, module connectors, cable connectors, and the component parts.
MIL-M-28787	Modules, Standard Electronic, General Spec for This specification establishes the quality assurance and procurement requirements for modules as defined in MIL-STD-1378 for the Standard Electronic Modules Program (SEMP) for use in military systems. Specific requirements for a particular module are listed in the detailed module specification.
MIL-P-28809	Printed Wiring Assemblies This specification covers conformally coated printed wiring assemblies (circuit-card assemblies) consisting of rigid wiring boards on which separately manufactured parts have been added.

MIL-M-38510	Microcircuits, General Spec for
	This specification establishes the general requirements for monolithic, multichip, and hybrid microcircuits and the quality and reliability assurance requirements which must be met in the acquisition of microcircuits. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended shall be specified in the applicable device specification. Multiple levels of product assurance requirements and control for monolithic and multichip microcircuits and two levels for hybrid microcircuits are provided for in this specification.
MIL-P-55110	Printed-Wiring Boards, General Spec for
	This specification establishes the <u>qualification</u> and <u>performance</u> requirements for rigid single-sided printed-wiring boards, rigid double-sided printed-wiring boards, and rigid multilayer printed-wiring boards with plated-through hole.
MIL-M-83436	Multiwire Interconnection Boards (Plated-Through Holes)

This specification has been superseded by IPC-DW-425, Design and End Product Requirements for Discrete Wiring Boards.

MIL-STDS

MIL-STD-275 Printed Wiring for Electronic Equipment

This standard establishes design requirements governing rigid, single-sided printed-wiring boards, double-sided printed-wiring boards, multilayered printed-wiring boards, printed-wiring assemblies constructed from those boards and design considerations for the mounting of parts and assemblies thereon. The design criteria (such as electrical spacings) contained in this standard are predicated on the requirement that end item assemblies (circuit card assemblies, printed-wiring assemblies, back planes, mother boards) shall be conformally coated in accordance with MIL-I-46058.

MIL-STD-454 Standard General Requirements for Electronic Equipment

This standard is the technical baseline for the design and construction of electronic equipment for the DOD. In one document, fundamental design requirements for 12 general electronic specifications are located.

DOD-STD-863	Wiring Data and System Schematic Diagrams, Preparation of This standard establishes the requirements for specific preparation and specific presentation of engineering data for aerospace vehicles and aerospace support applications. This engineering data (wiring data and schematic diagrams) is to be used for (1) configuration control by management activity, (2) direct incorporation into technical publications without redrawing, (3) training of maintenance personnel, and (4) development of engineering source document for fault isolation logic and analysis.
MIL-STD-1378	Requirements for Employing Standard Electronic Modules This standard provides equipment contractors with specific direction for the implementation of the Standard Electronic Modules Program (SEMP) and reduction of system life cycle costs. Use of this document should be based upon the criteria of MIL-HDBK-246 and the design requirements of MIL-STD-1389.
MIL-STD-1389	Design Requirements for Standard Electronic Modules

The purpose of this document is to establish the general design requirements for Standard Electronics Modules (SEM), herein termed modules, for use in military systems. Other requirements for new module development are contained in MIL-STD-1378. The modules shall be designed to satisfy the quality assurance requirements of MIL-M-28787 for the appropriate class selected to meet the system/equipment environmental requirements.

MIL-STD-1472 Human Engineering Design Criteria for Military Systems, Equipment and Facilities

This standard establishes general human engineering criteria for design and development of military systems, equipment and facilities. Its purpose is to present human engineering design criteria, principles and practices to be applied in the design of systems, equipment and facilities so as to:

a. Achieve required performance by operator, control and maintenance personnel,

b. Minimize skill and personnel requirements and training time,

c. Achieve required reliability of personnel/equipment combinations,

d. Foster design standardization within and among systems.

MIL-STD-1553 Aircraft Internal Time Division Command/Response Multiplex Data Bus

This standard establishes requirements for digital, command/response, time division multiplexing (data bus) techniques on aircraft. It encompasses the data bus line and its interface electronics and defines the concept of operation and information flow on the multiplex data bus and the electrical and functional formats to be employed. Even with the use of this standard, subtle differences will exist between multiplex data buses used on different aircraft due to particular aircraft mission requirements and the designer options allowed under this standard.

MIL-STD-1589 JOVIAL J73

This standard establishes the higher order language (HOL) and associated tool set for JOVIAL J73.

MIL-STD-1629	Procedures for Performing a Failure Mode, Effects and Criticality Analysis This standard establishes requirements and procedures for performing a failure mode, effects and criticality analysis (FMECA) to systematically evaluate and document, by item failure mode analysis, the potential impact of each functional or hardware failure on mission success, personnel and system safety, system performance, maintainability, and maintenance requirements. Each potential failure is ranked by the severity of its effect in order that appropriate corrective actions may be taken to eliminate or control the high risk items.
MIL-STD-1634	Module Descriptions for the Standard Electronic Modules Program This standard contains synopsis descriptions of Standard Electronic Modules as specified in MIL-M-28787. It provides a listing by key code of the existing SEM modules designed in accordance with MIL-STD-1389 and MIL-M-28787.
MIL-STD-1665	Test Equipment for the Standard Electronic Modules Program This standard establishes the capabilities of electronic test equipment

needed for testing of Standard Electronic Modules (as specified in MIL-M-28787). It specifies equipment performance parameters and lists representative test equipment.

MIL-STD-1750	Sixteen-bit Computer Instruction Set Architecture

This document establishes and defines a uniform instruction set architecture (ISA) for airborne computers which shall be used in Air Force avionic weapons systems. .....the ISA is applicable to and shall be used for computers that perform such functions as moderate accuracy navigation, computed air release points, weapon delivery, air rendezvous, stores (armament) management, aircraft guidance, and aircraft management.

DOD-STD-1788	Avionics Interface Design Standard

This standard defines the form factor, mounting, and cooling criteria to be used for military Line Replaceable Units (LRU's) and the associated equipment rack. Specific dimensions and environmental characteristics govern the design of new and repackaged standard electronic equipment that is intended to be installed in the equipment bays of military aircraft.

MIL-STD-1815 Ada

This standard defines the Ada Higher Order Language.

MIL-HDBKS

MIL-HDBK-217 Reliability Prediction of Electronic Equipment

This handbook establishes uniform methods for predicting the reliability of military electronic equipment and systems. It provides a common basis for reliability predictions of military electronic systems and equipment under acquisition as well as for comparing and evaluating reliability predictions of related or competitive designs.

MIL-HDBK-246 Program Managers Guide for the Standard Electronic Modules Program

This handbook covers the relevant phases of an equipment development program which would be impacted by the decision to implement equipment hardware requirements with SEM. It provides the necessary guidance for determining the initial applicability of SEM for military system applications, as well as for evaluating and monitoring those aspects of a program once a contractual requirement has been established. It specifically assists the program manager:

a. In assessing the cost impact of SEM versus non-SEM electronic equipment implementations,

b. In preparing the appropriate SEM requirements within system acquisition documents,

c. In establishing a methodology for evaluating SEM configured system proposals,

d. In establishing an orderly procedure for operating and coordinating with SEMP support activities,

e. In monitoring the SEMP milestones within a system development program.

MIL-HDBK-472 Maintainability Prediction

This handbook is to familiarize managers and engineers with maintainability prediction procedures applicable solely to electronic systems and equipments and includes only those procedures which are currently used in the prediction process. Maintainability prediction facilitates an early assessment of the maturity of the design and enables decisions concerning the compatibility of a proposed design with specified requirements or the choice of better alternatives. It includes procedures for the prediction of maintainability of electronic systems at the organizational, intermediate and depot levels of maintenance.

APPENDIX B

TESTABILITY

LRM Test and Maintenance Technology

<u>TRW Approach.</u> The TRW approach includes the use of a maintenance processor. The maintenance processor function is to direct test inputs (vectors) and to acquire and compare output vectors from a family of chips to predicted values, or sets. In phase I VHSIC, the maintenance processor will be located off the chip and will be responsible for a number of chip families with each functionally partitioned set contained on a single LRM. The maintenance processor will interface with each VHSIC/Semi-custom chip through a maintenance node which serves as a terminal for the maintenance network. The maintenance bus between the processor and each chip will be a dedicated bus which is segregated from operational buses. Each family will be controlled and monitored through a separate channel in the maintenance processor. In phase II VHSIC, the maintenance processor will be a subset of each chip and will serve to detect failures within the device and to reconfigure macrocells around faults. The maintenance processor architectures shown in figures B-1 and B-2 show the TRW phase I VHSIC approach. Modules in this test scheme rely on off-module maintenance processors interfacing through a module maintenance node.

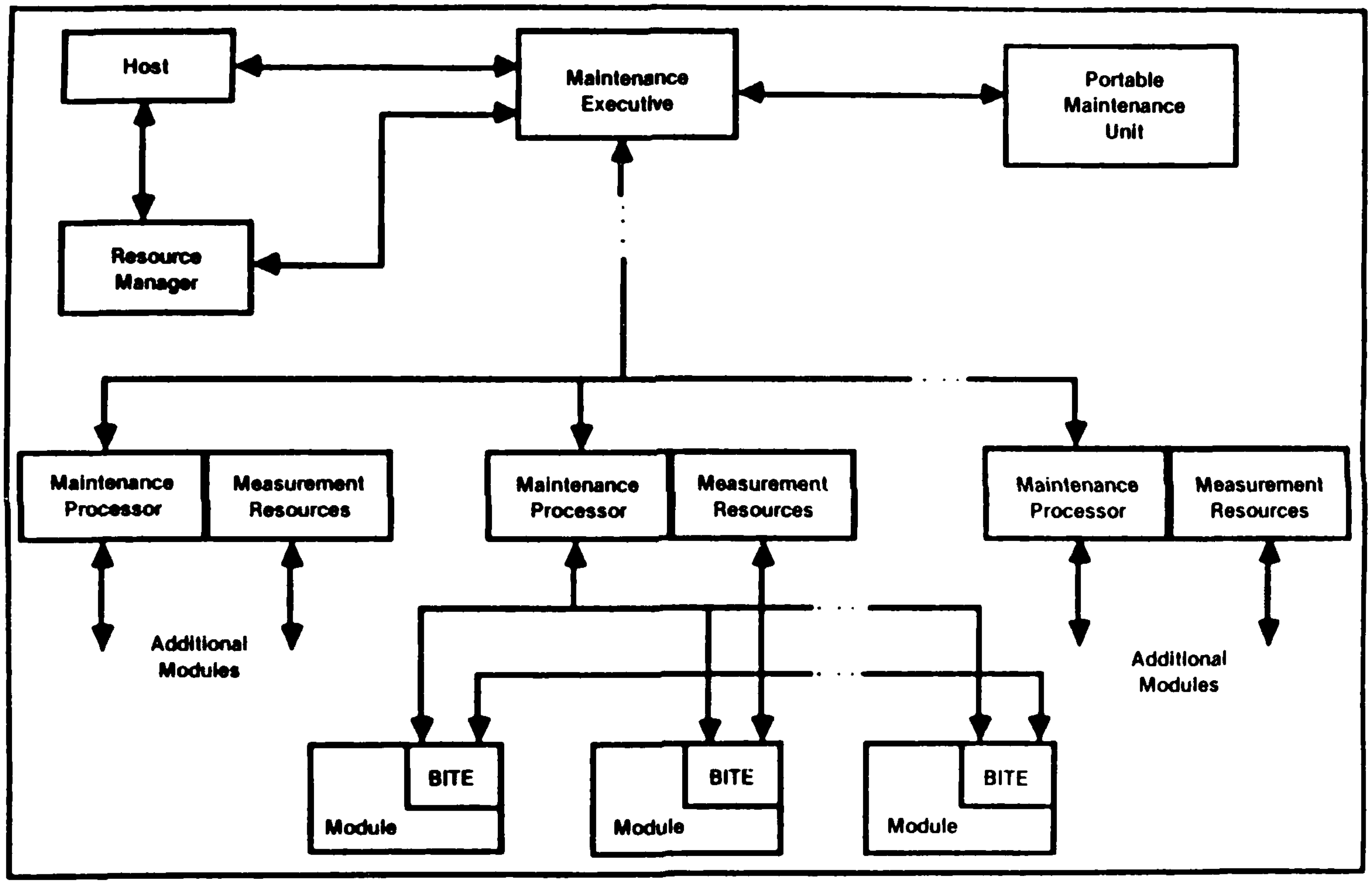


Figure B-1. Maintenance and Diagnostic System

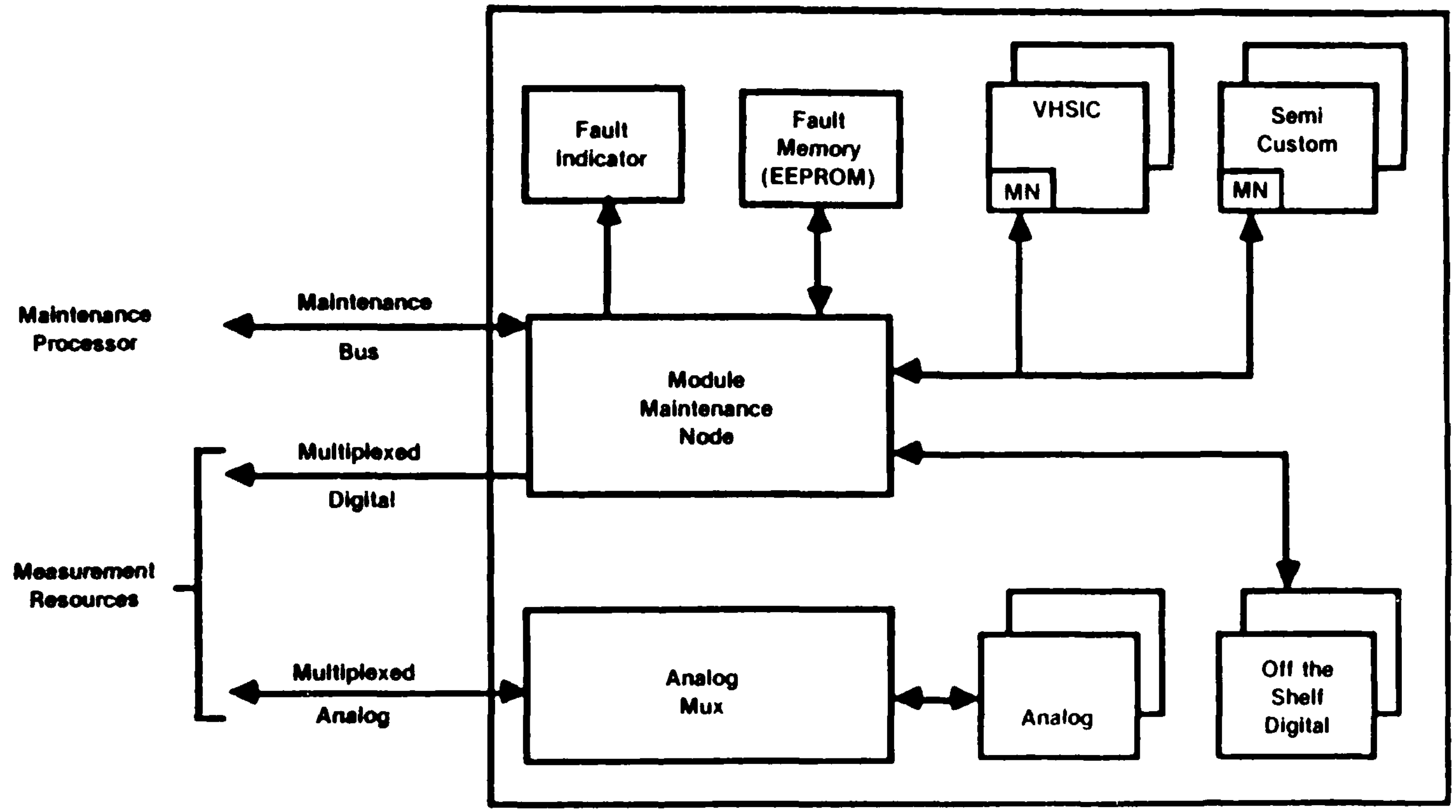


Figure B-2. Module Built-In Test Equipment

Westinghouse Approach. System architecture requirements as defined for the Advanced Tactical Fighter include the capability of autonomous board level BIT. To perform on-board testing of the Westinghouse ATF advanced systems module suite through a hierarchical scheme, a Module Maintenance Processor (MMP) is under development for each SRU. Utilizing a VHSIC processor, the MMP will control the loading of test vectors or seed vectors from EEPROM into the operational circuitry. The MMP (refer to figures B-3 and B-4 below) will also control the loading of TSMD and fault data into a non-volatile memory. Interface with other modules will be through the standard serial Test/Maintenance (T/M) bus and/or the Parallel Interface (PI) bus.

The MMP will contain non volatile memory (NVM) or seed vector storage, fault code/TSMD data (fault signature), and test/maintenance algorithms. Random access memory (RAM) will reside in the MMP architecture to accept fault and stress data continuously until a threshold is reached. Once a stress threshold is reached and/or a failure verified, the RAM volatile memory contents will be loaded into the NVM. Chip to MMP interface will be through the Extended Test/Maintenance (ETM) bus which is a VHSIC phase II standard under promulgation. Glue chip and analog circuitry will require analog to digital (A/D) converters which will also reside in the MMP.

The MMP will require start-up testing to "test the tester". The system resource manager upon start-up will initiate MMP test. MMP communication over the T/M and PI bus is considered a primary initializing test.

FLIGHT LINE MAINTENANCE VHSIC SYSTEM

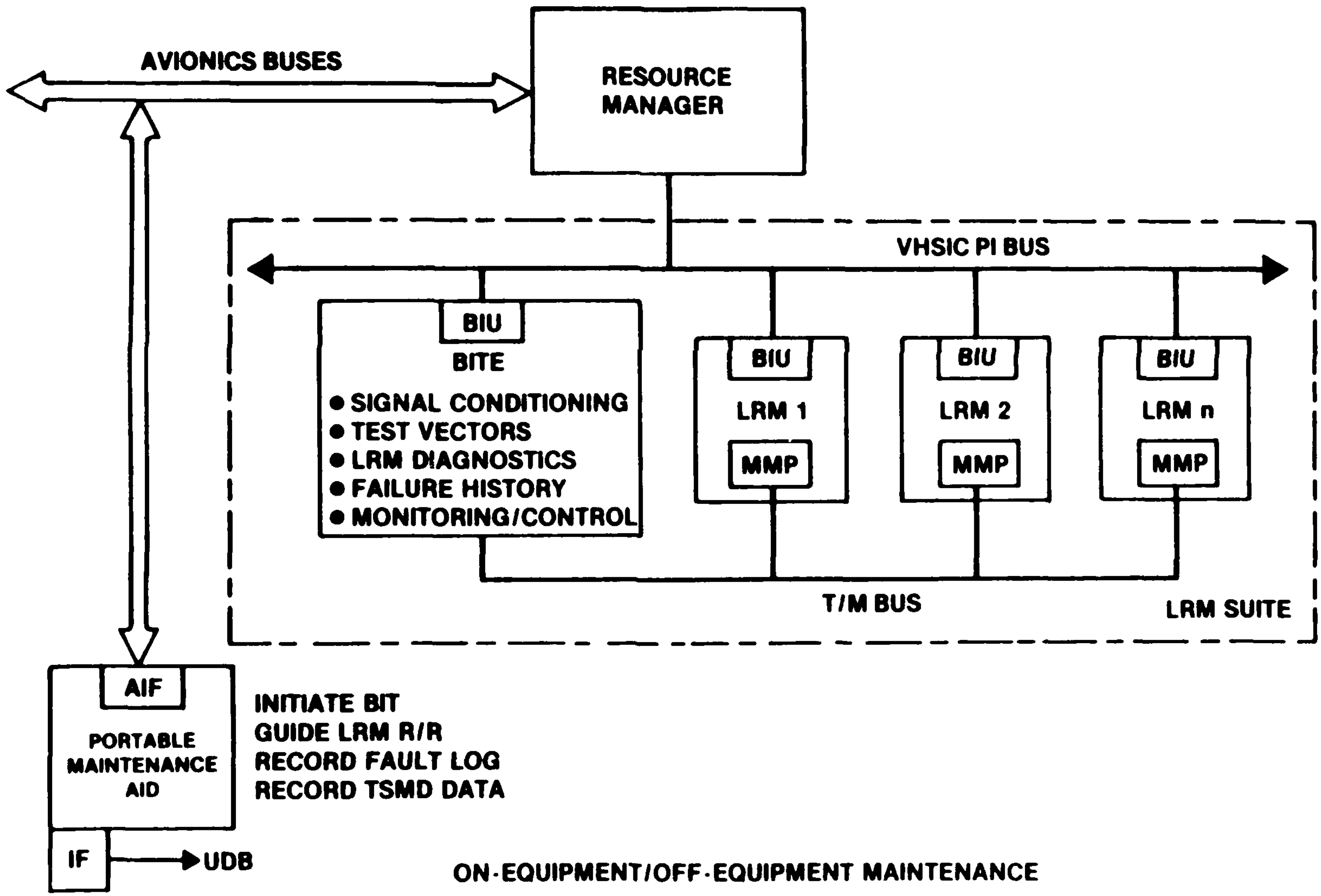


Figure B-3. MMP LRM Integration

MMP — FUNCTIONAL CONFIGURATION

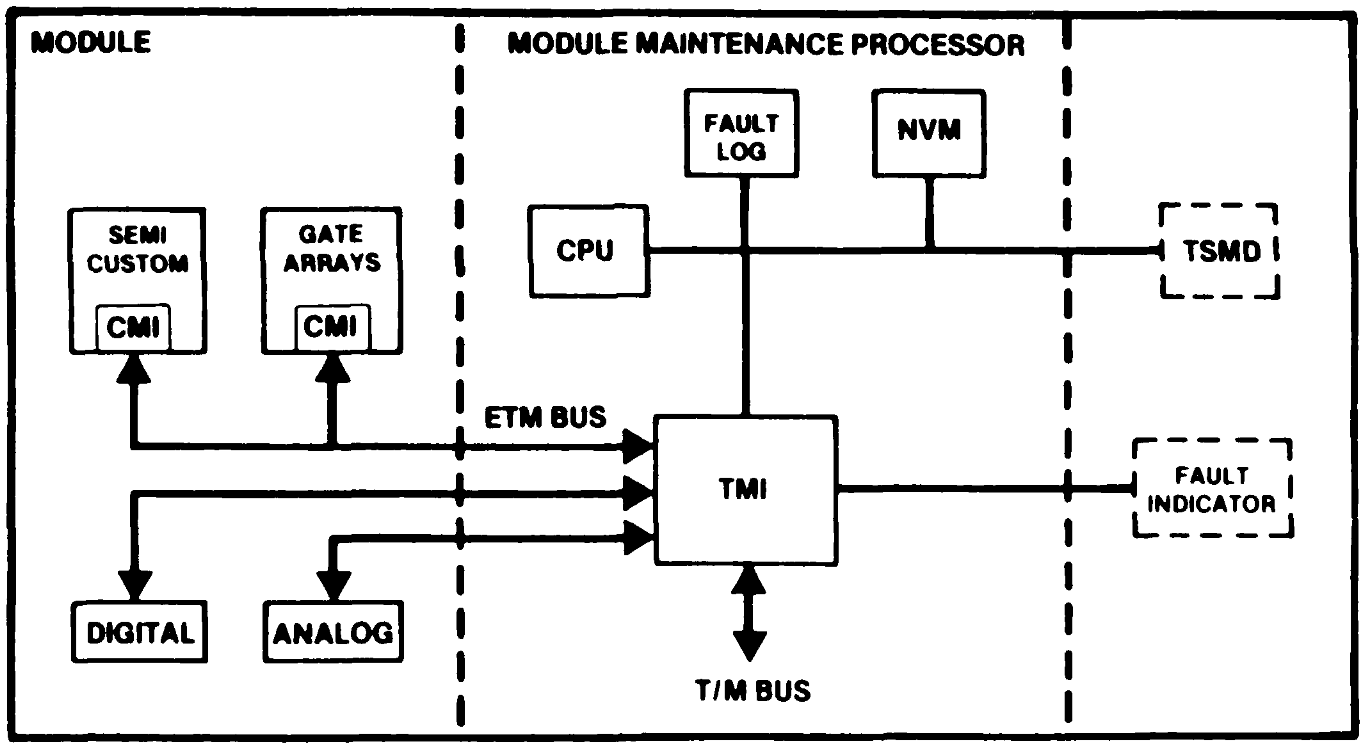


Figure B-4. MMP Architecture

Honeywell Electro-Optical Signal Processor (EOSP) Approach. The EOSP phase I VHSIC chip set consists of a Sequence Chip, an Arithmetic Chip, and a Parallel Programmable Pipeline (PPP) Chip. The intended use of the EOSP is for automatic target acquisition real-time image processing algorithms . An array of 32 PPP chips are controlled by a single control pair consisting of a sequencer and arithmetic chip (refer to Figure B-5). The sequencer serves as a maintenance controller and contains both a test vector generator and a signature generator. The PPP chip contains only a signature generator; therefore, signature analysis testing of a PPP can be controlled by the Sequencer chip. The Arithmetic chip uses the signature analyzer in the sequencer chip.

The test interface logic of the sequencer chip is designed to enable a "hard core" section of the sequencer chip to perform a self-test of the balance of the sequencer and arithmetic chip, and of any PPP chips connected to it. The architecture of the sequencer is shown in Figure B-6. The Sequencer interfaces to the subsystem maintenance controller through the Test/Maintenance bus.

Phase II VHSIC efforts by Honeywell include the incorporation of maintenance controllers on each chip with a standard ETM bus interface. Test Maintenance Controllers will interface with a module test/maintenance processor (TMP) as shown in figure B-7.

Testability schemes. Testability schemes for VHSIC phase 1 and 2 technology are embodied in the DoD lead Design For Testability (DFT) requirement. DFT is the result of an iterative process between the logic design and test vector generation. The same test point accessibility usingg a gate

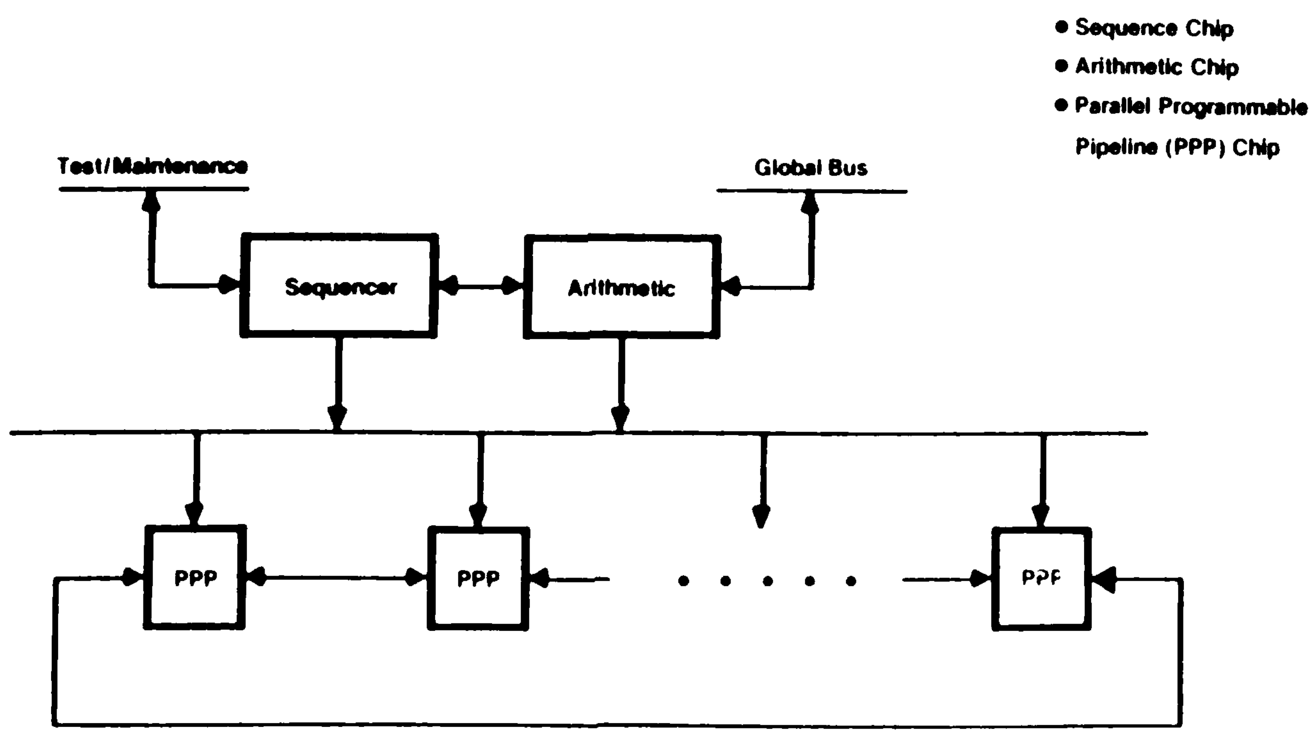


Figure B 5. EOSP Architecture

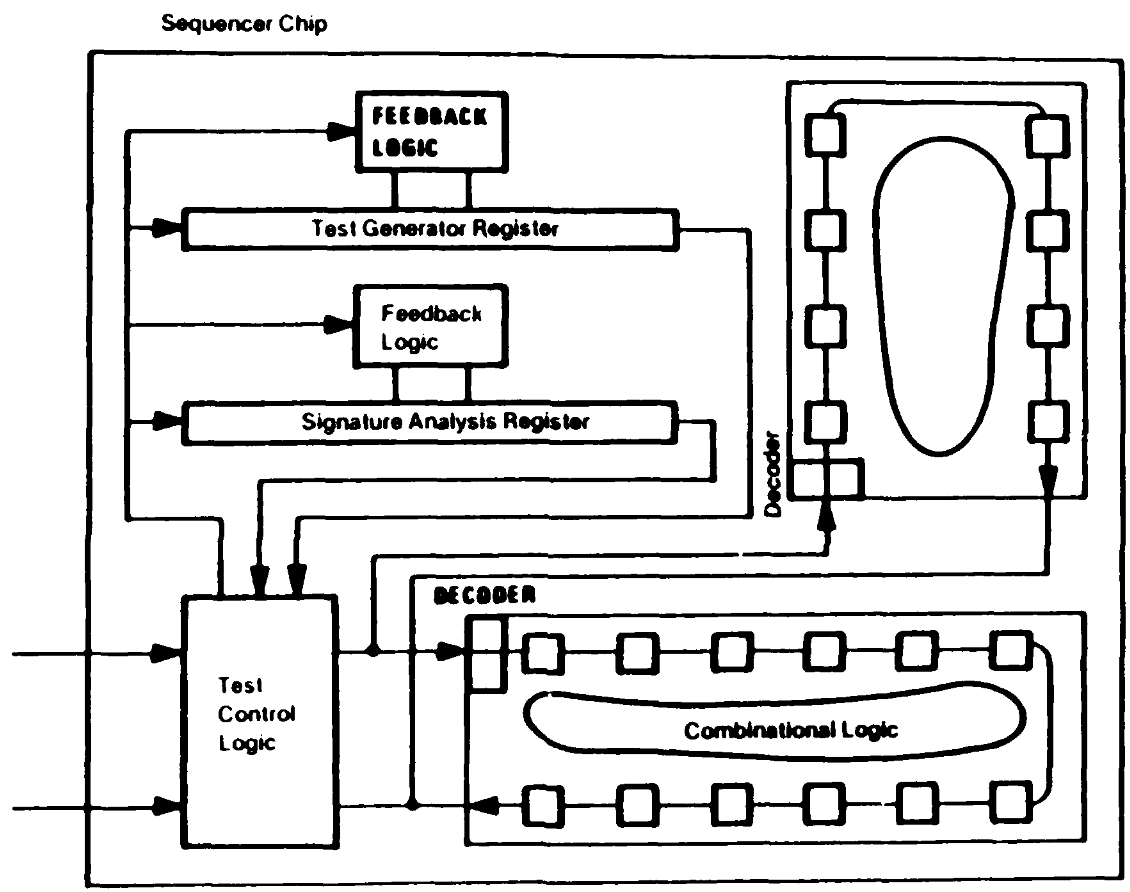


Figure B-6. Sequencer Architecture

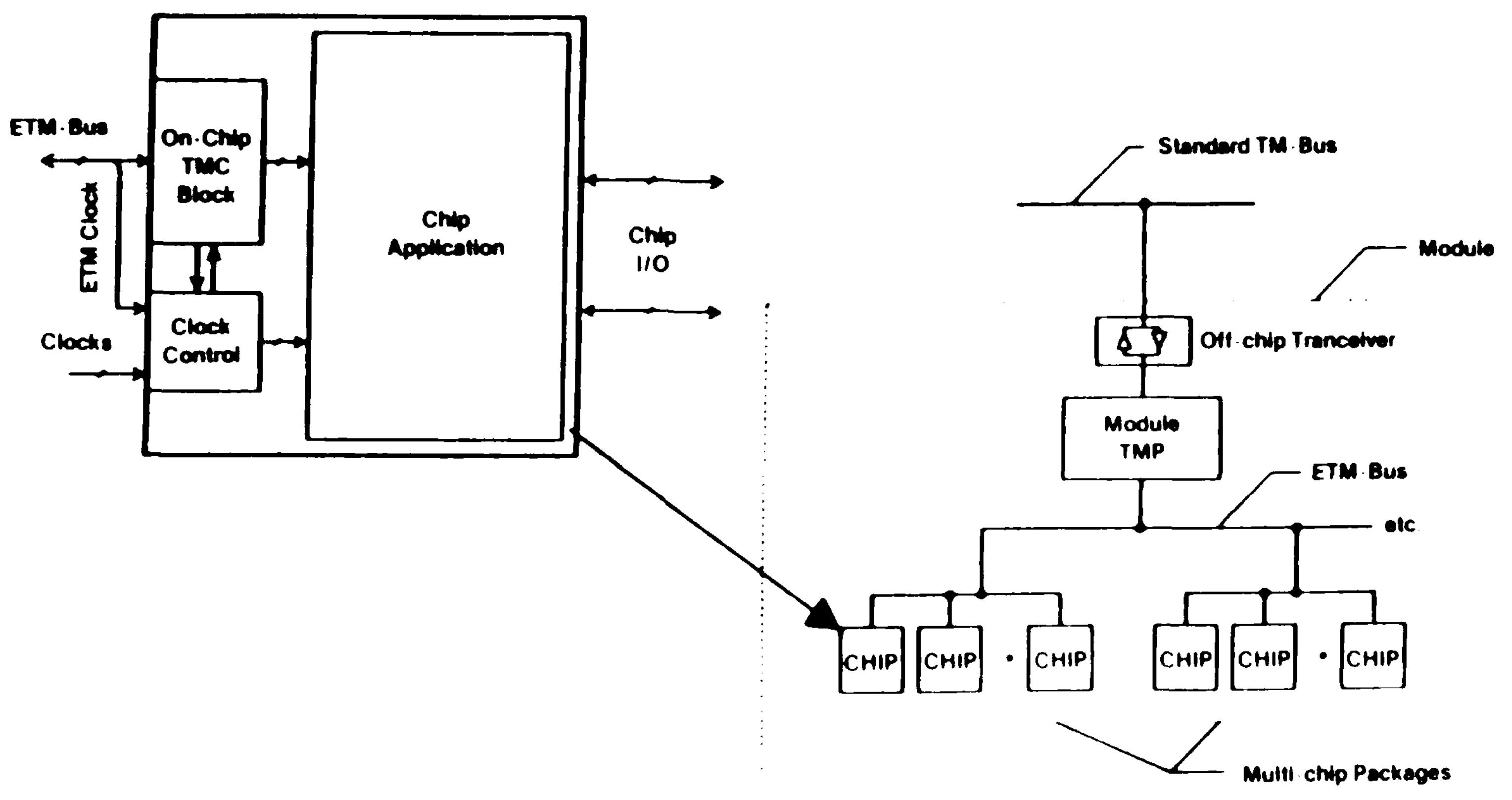


Figure B-7. Phase II VHSIC LRM Testability level simulation is not possible with a physical VHSIC chip. Logic designs are subsequently modified to include circuit inputs and outputs to provide control of the test vectors and observability of the results. Added on-chip test logic and external test nodes may increase chip area by 20 percent. Phase 1 and 2 VHSIC chips with gate densities ranging from 4000 gates to 500,000 gates per device, respectively, can allow for test/maintenance nodes on each chip. Chip level test schemes include non-intrusive signature analysis and boundary scan techniques. Intrusive, off-line techniques include level sensitive scan design (LSSD).

Signature Analysis testing of a chip is accomplished by generating pseudo random vectors to be applied to subsection inputs, and sending each corresponding output to a signature analysis register. After applying a predetermined number of test vectors, the contents of the signature analysis register is compared with the known correct signature. This technique relies on external application of test vectors. Test vectors can be pseudo-randomly generated via a seed vector set. A seed vector set can be resident on-module in non-volatile memory. Pseudo random test vector generation on-module relies on a maintenance controller. Test vectors can be downloaded from external sources such as depot ATS. Signature analysis is a non-intrusive test scheme which verifies chip function externally. Scan test techniques are required to test deeply embedded chip logic.

The most popular scan test techniques include level sensitive scan design and boundary scan. In the test mode, all internal memories are chained together into one or more shift registers referred to as scan-chains. Chip logic whose inputs are fed by a scan-chain and whose outputs feed a scan-chain is designated interior logic. Combinational logic whose inputs are fed by primary inputs or outputs are designated exterior logic. If all primary inputs and primary outputs are placed in a scan-chain then there is no exterior logic. Such a scan-chain connecting all primary I/O is called a boundary scan. Level sensitive scan design (LSSD) uses specially designed two-part shift register latches (SRLs) in conjunction with the circuit combinational logic to provide a scan path through each device. Deeply embedded logic can be accessed and exercised by shifting data through the SRLs to the combinational logic where it can be clocked through to the output and compared. This scan technique is intrusive (does not support concurrent testing) to operational use of the device.

APPENDIX C

TECHNOLOGIES

Device Technology

Phase I VHSIC. Six companies and industrial teams that were funded for phase 1 contracts have fabricated approximately 30,000 operational microcircuits. The contractors include: Honeywell; Hughes Aircraft; IBM; Texas Instruments; TRW; and, Westinghouse. Major yield enhancements have been realized for several chip types including: the Honeywell Sequencer, containing 136,000 devices with a yield of 25%; the Texas Instruments 72K static ram containing 465,000 devices with a yield of 69%; the Westinghouse 65K static ram containing 400,000 devices with a yield of 25%; and the TRW Window Addressable Memory containing 58,000 devices with a yield of 20.5%. Initial yield projections for these and all of the remaining phase 1 devices was in the 12 - 15 percent range. Cost effective yields in excess of 15 percent are primary candidates for military usage in the near future.

The following list is a matrix containing vendors, chip types, technology employed, and packaging arrangement.

Vendor	Chip Name	Technology	Packaging
Honeywell	Sequencer	Bipolar	multilayer ceramic 180 pin array, 1.45 x 1.45 inches, 12 mil pitch pads

Vendor	Chip Name	Technology	Packaging
	Parallel Prog Proc	same	same
	Arith Device	same	same
Hughes	Sig Track Subsystem	CMOS/SOS	148 pin leaded ceramic chip carrier, 25 mil center leads, 1.0 x 1.0 inches
	Algebraic Encoder/decoder	same	same
	Digital Correlator	same	same
	8K CGA	same	same, customized to application
	EOSP Control	same	180 pin ceramic pin array, 1.575 x 1.575 inches
IBM	CMAC	NMOS	240 pin ceramic pin array, 2.165 x 1.56 inches
	Sig Proc Element	same	100 pin array, 1.10 x 1.10 inches or 144 pin mil spec pin grid array
TI	Vector Arith/ Logic Unit (VALU)	Bipolar	64 pad leadless chip carrier (LCC), 1.15 x 1.15 inches
	Array Controller/ Sequencer (ACS)	same	84 pad LCC, mil center pads, 1.15 x 1.15 inches
	Vector Address Generator (VAG)	same	same

Vendor	Chip Name	Technology	Packaging
	Multipath Switch (MPS)	same	same
	Data Processor Unit (DPU)	same	same
	Device Interface Unit (DIU)	same	same
	General Buffer Unit (GBU)	same	same
	Static RAM (SRAM)	NMOS	32 pad LCC, 50 mil center pads, 0.45 x 0.55 inches
TRW	Register Arithmetic Logic Unit	Bipolar	132 pad LCC, 25 mil center pads, device wire bonded to package
	Address Generator	same	same
	Multiplier Accumulator	same	same
	Content Addressable Memory	same	same
	Matrix Switch	same	same
	Microcontroller	same	same
	Four Port Memory	Bulk CMOS	same
	6K Gate Array	same	same
	Convolver Decoder Bipolar	1.0 micron	same
	FFT Arith Unit	Bulk CMOS	same
	FFT Control Unit	same	same
	32 Stage Convolver		same same

Vendor	Chip Name	Technology	Packaging
	Window Addressable Memory	Bipolar	same
Westinghouse	General Purpose Controller	Bulk CMOS	ceramic 224 leaded chip carrier, 20 mil pitch leads, 1.25 x 1.25 inches
	Extended Arith Unit	same	same
	Pipelined Arith Unit	same	same
	Extended Arith Unit Multiplier	same	same
	64K Memory	same	42 pin ceramic leaded chip carrier, 20 mil pitch leads, 0.55 x 0.70 inches
	10K Gate Array	same	164 pin leaded chip carrier, 20 mil pitch leads, 0.95 x 0.95 inches

EOSP - Electro-Optical Signal Processor
CMAC - Complex Multiply and Accumulate

Each chip in the TRW chip set contains a Maintenance Network Node (MNN) which interfaces with the Maintenance Network Processor (MNP) through a dedicated test bus. Each Westinghouse device uses a BIT macro which is used for chip test through a dedicated maintenance bus.

Phase II VHSIC. Phase 2 microcircuits are devices which have submicron (0.5 micron) feature size, operate at clock speeds of 100 Mhz, and are to have at least 100,000 gates for chip sizes of about 0.350 x 0.350 inches. Three phase 2 contractors were selected to follow phase one 1.25 micron technology. They include TRW, IBM, and Honeywell.

TRW is using Bipolar and CMOS technology to develop three "superchips" with three additional option devices. They include:

High Speed General Purpose Signal Processor capable of 400 million complex operations per second (MOPS) which is 1.4 x 1.4 inches. This device is CMOS and contains 28 million devices.

Convolver Correlator capable of 13 billion operations per second (BOPS). This 1.4 x 1.8 chip is designed in bipolar technology and contains 10 million devices.

Mass Memory which is a four port type with capacity of 64K words. This CMOS device is a 1.4 x 1.8 inch superchip containing 28 million devices.

Fast Fourier Transform (FFT) chip which is a 1024 point bipolar device which operates at 1 BOPS. This 1.4 x 1.4 inch device contains four million devices.

High Speed General Purpose 32 bit Data Processor Chip designed to operate at 20 million instructions per second (MIPS) and which will contain a one megabit memory. This CMOS device measures 1.4 x 1.8 inches and contains 35 million devices.

Associative Processor device designed to perform associative matches at a 10 BOPS rate. This 1.4 x 1.4 inch CMOS superchip contains 10 million devices.

Honeywell is developing configurable gate arrays (CGAs). Honeywell will devote a portion of their CGA to standard macrocells with the remainder of the chip containing tailored cells for a specific application. Using Bipolar technology, Honeywell is developing the following devices:

Array Processor containing 30,000 logic gates with 8K of RAM. This Bipolar device includes 284,000 devices.

Array Processor Controller Chip.

System Interface Chip for a standard input/output data bus.

Deduced Instruction Set Computer.

Enhanced Bus Interface Unit.

Honeywell will mount phase 2 chips in multichip carriers providing 420 input/output pins

IBM is developing a phase 2 chip set using CMOS technology of 0.50 micron feature size. IBM devices include:

Systolic Processor.
Configurable Static Random Access Memory.
Bus Interface Unit.
Address Generator (1.0 micron feature size)

The IBM approach to packaging is similar to the Honeywell implementation. IBM will use a 2.5 x 2.5 inch enclosure containing 16 uncased phase 2 chips. Each package will contain 500,000 gates or 7 million devices.

APPENDIX D

MASA

Modular Avionic System Architecture (MASA) Air Force Regulation 800-45

MASA establishes the logistics support concepts necessary to support an integrated avionics system. The MASA concept applies to advanced avionics included in: aircraft and missiles; subsystems within the Pave Pillar/Pave Sprinter advanced system architectures (ASAs); and insertion efforts such as the replacement of individual line replaceable units (LRUs) within mature systems such as the F-15 Central Computer.

The integrated support process is detailed in figure D-1.

MASA outlines supportability design drivers for On-Board Aircraft systems, Base Support, and for Depot Maintenance. Technology and methodology drivers which are directly applicable to VHSIC Automatic Test Systems (ATS) have been excerpted from the MASA document and will be addressed in subsequent sections.

<u>On-Board Aircraft.</u> On-board aircraft system architecture will be divided into the operational and non-operational elements. Operational elements include Subsystem Executives with their test/maintenance link and system Resource Management. A non-operational element included is the Data Transfer System.

MASA INTEGRATED SUPPORT PLAN

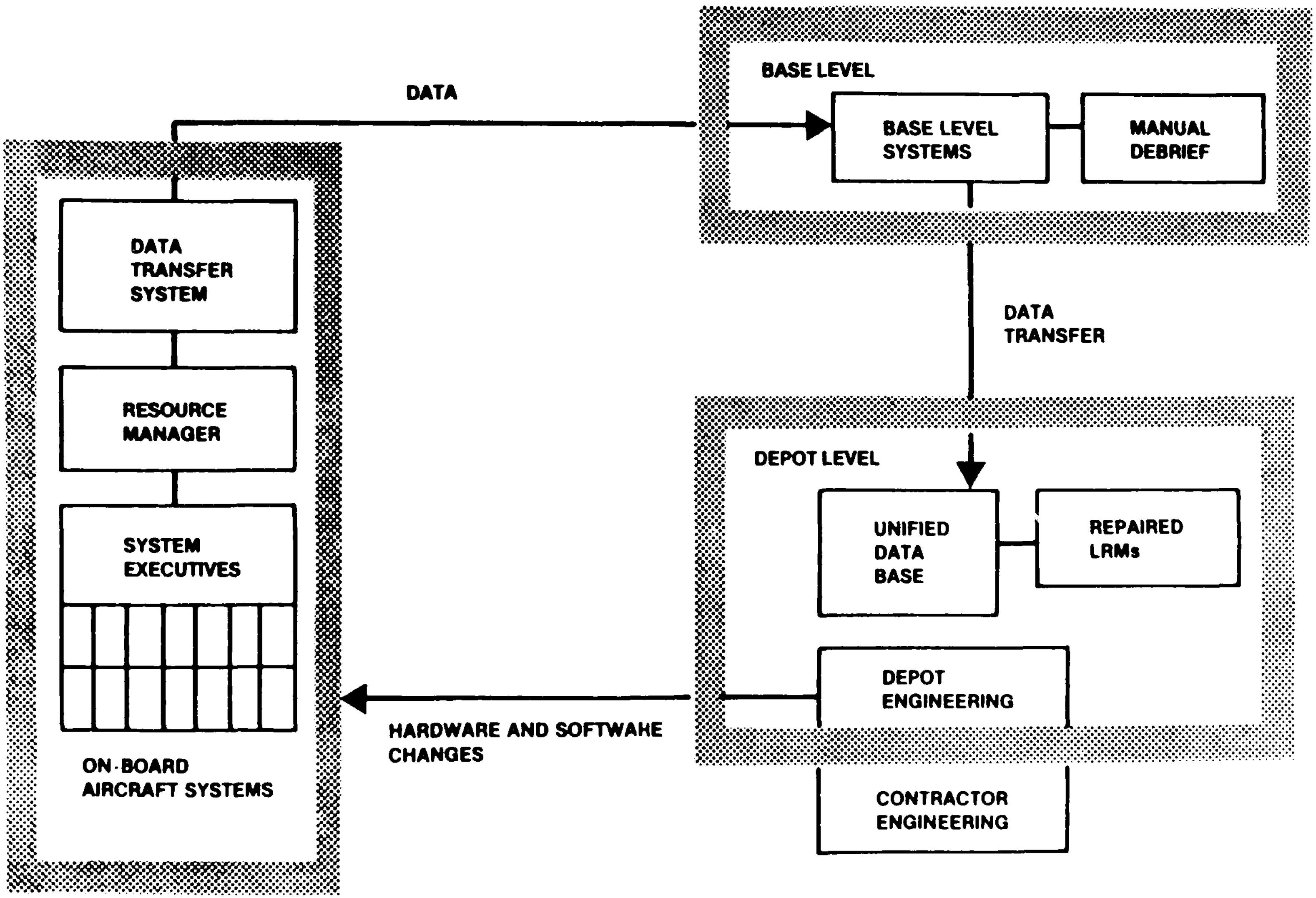


Figure D-1

Subsystem Executive. Each subsystem is composed of Line Replaceable Modules (LRMs) with autonomous maintenance capabilities. LRMs may be standard, common, or unique. Standard modules meet the requirements of a specific standard established by at least one DoD group and is useable on any system requiring that standard (ie. 1750A Instruction Set Architecture Processor Module). Common modules are those already in use in multiple applications. Unique modules include those LRMs which are used within a single subsystem only. Each subsystem executive which performs a control function for the subsystem, manages the subsystem resources (ie. on-module reconfiguration), and communicates as required with other system or subsystem software.

Resource Manager. The resource manager controls all MASA system resources and serves to reassign subsystems around critical failures. The resource manager responds to operational mode requirements as directed by the pilot/ operator. This function which resides at a hierarchical level above the subsystem executive also has access to history of all system failures during the mission. The resource manager is responsible for fault data formatting for subsequent downloading through the Data Transfer System (DTS).

DTS. As the name implies, the DTS is responsible for data transfer through one of three mechanisms:

Data Link	aircraft downlink prior to aircraft landing.
Data Transfer Cartridge (DTC)	Memory cartridge presently used on the F-16 C/D to download fault information.

Aircraft Bus/ Maintenance Device	Portable support equipment access through the aircraft 1553B or High Speed Data Bus to the resource manager.

Base Level Support. Fault/Maintenance data in the base level information system is used in conjunction with manual pilot de-briefing to aid maintenance personnel in returning aircraft to operational status. This data includes all fault codes, parameter values (operational scenario time stamp), and Time Stress Measurement Device (TSMD) data. This data will be loaded into a Unified Data Base (UDB) for subsequent analysis. Access to the UDB will give the base commander the ability to project system availability through trend analysis. In addition, prognostic or pre-emptive maintenance can be performed based on statistical analysis.

Depot Maintenance. The depot will have responsibilities which include large scale failure trend analysis through the UDB, LRM and chip testing, LRM repair, and contractor interface. Depot personnel will be responsible for updating rule based artificial intelligence (AI) programs which will be exploited by base level commands to diagnose multiple systemic failures. Presently, the Integrated Maintenance and Information (IMIS) Program underway through Pave Pillar and the Wright-Patterson Human Resource Laboratories will drive the implementation of the UDB. Failure trend analysis will also serve to accelerate depot fault isolation and repair. In addition to LRM/Chip level testing, the depot will be responsible for module repair. A critical element of the MASA integrated support plan will include depot liaison with LRM and chip manufacturers to drive hardware and software changes to enhance system reliability and maintainability.

UDB. The UDB will provide the basis for a closed loop feedback system. Software support will be managed through the unified data base. The UDB will be a distributed network consisting of design and logistics data bases and integrated analysis tools which includes a Tester Independent Software Support System (TISSS) interface. A critical element of the UDB will be vendor design data. Vendor design data will consist of computer aided design/engineering/manufacturing (CAE/CAE/CAM) information in addition to simulation and test specification data. Included in software support are the automatic test equipment (ATE) support tools such as TISSS and the VHSIC Hardware Description Language (VHDL).

Source data for MASA ATE shall be a part of the UDB. LRM and chip model libraries, source code and object code of the ATE test programs (hardware/software configuration management), and unit under test (UUT) software development will be managed through the UDB.

Avionics Maintenance and Test

Direct On-Equipment Maintenance. On-Line and Off-Line Built-In-Test (BIT) will detect and isolate avionics system faults. Following easy access and removal of a faulty subsystem (ie. LRMs), on-equipment BIT will be initiated to verify operational integrity. Integrated racks containing backplanes, LRMs, wire and fiber optic bundles, and cooling components are subject to on-equipment fault isolation. As such, hierarchical BIT controlled through the system resource manager will assist the technician in identifying and repairing faulty subsystems. Faulty subsystems will be returned to the depot for repair. For system failures beyond on-equipment repair, the rack containing N LRMs and the backplane will be removed for off-equipment maintenance.

Direct Off-Equipment Maintenance. MASA items will not have off-equipment (Intermediate level) support equipment to verify aircraft on-equipment fault detection.

Off-Equipment Depot Maintenance. LRMs will removed and replaced at the aircraft. Without intermediate fault isolation or verification, LRMs will be sent to the LRM Repair Facility (LRF). The LRF will test and repair LRMs and sub-assembly hardware. The LRM hardware shall be repaired by removal and replacement of faulty components/devices, connectors, or printed circuit boards. Hardware redundancy may be activated by device reconfiguration. ATE and environmental support equipment will be necessary for LRM and chip testing. The LRF will repair faulty LRMs using standardized test procedures (TISSS product), exercise LRM and chip reconfigurability, and perform verification testing on ATE.

MASA ATE for depot must test digital, analog, RF, and microwave electronics. MASA ATE will interface with LRM maintenance processors for BIT access. LRM level ATE will test at operational clock speeds, simulate environmental stresses discerned from LRM TSMDs, and must test VHSIC and non-VHSIC (glue chips) of various technologies. In addition, the depot must test chips with automatic microcircuit test equipment exploiting UDB/TISSS interfaces.

The unit-under-test (UUT) will be tested under the same conditions experienced in the weapon system at failure. The attributes of the ATE required to accomplish this include: high speed multiple clocks; large memory size; accurate timing; interface compatibility; fault coverage; sufficient signal level dynamic range; go/no go test; and, end-to-end test. Ancillary equipment such as ovens, freezers, and vibration equipment will be necessary.

On/Off Line Testability

On-line and Off-line BIT programs resident in the MASA system shall isolate unambiguously to a single item not less than 98 percent of the detected faults. On-line automatic BIT will be non intrusive to system operation and will have a 96 percent fault detection capability of all faults which affect system performance. For all LRM detected failures, fault codes, parameter values, signal operations values, and TSMD data shall be recorded on the LRM. Off-line BIT diagnostics which are operationally intrusive will be used to fault isolate to a faulty item when on-line BIT fails to detect or isolate a problem. Off-line BIT diagnostics will be performed through an fighter aircraft system bus using appropriate support equipment.

On-LRM Testability

MASA requires a structured approach for testing. Hierarchical testing from chip to module to subsystem to system will be required. Each chip shall communicate test and maintenance (T/M) data chip-to-chip and module-to- module over standard buses with standard protocols. These common test interfaces assure common chip-to-chip and module-to-module interoperability irrespective of their manufacturer.

The LRM maintenance controller will control the exchange of T/M data, on-chip BIT in on and off line modes, at-speed test of chip drivers and interchip connections, test of backplane interconnections between LRMs, and chip clock timing. The maintenance controller will also exchange repair validation data with the UDB. The LRM maintenance controller will also perform fault detection and fault diagnosis testing on hybrid packages and glue chips that do not have test registers. The LRM maintenance controller must support dynamic reconfiguration at the chip and/or module level where active redundancy is available.

APPENDIX E

DATABASE SORT

1.0 Testability/On-Module BIT Processor - Sort 1

Sort 1 defines the following records:

- o MOD_FUNC — Module function.
- o VENDOR — Module Producer.
- o TEST_SCHM — Testability scheme(s) employed on module
- o OCLK_MOD — Does the module have an on-board clock?
- o OPROCOP — Does the module have an on-board processor for operational use (smart module).
- o OPROCBF — Does the module have an on-board processor dedicated to autonomous module test.

1.1 Observations

The purpose of this sort was to illuminate whether autonomous test processors were being designed into operational circuitry. Sixty-two percent of the modules identified did not have maintenance processors. Testability schemes for module VHSIC/VLSI devices showed a predominance of serial scan techniques, both set scan and boundary scan. These were combined with signature analysis to provide total device testability. Significant use of on-chip test vector generation using psuedo-random TPG from seed vectors was also apparent.

2.0 Autonomous Module Maintenance Processor - Sort2/2A

Sort 2 defines the following records:

- o MOD_FUNC — Module function.
- o VENDOR — Module Producer.
- o OPROCBF — Does the module have an on-board processor dedicated to autonomous module test.
- o OPROCBFCR — Details of on-board processor dedicated to module test.

Sort 2A, Module Maintenance Processor/Bus Interfaces, defines the following records:

o MOD_FUNC	Module function.
o VENDOR	Module Producer.
o OPROCBF	Does the module have an on-board processor dedicated to autonomous module test.
o INTFC	Bus Interfaces to LRM

2.1 Observations

The population of modules having on-module maintenance processors was limited. Several maintenance processors exercise the 1750A instruction set architecture (ISA).

3.0 Bus Interface Standardization - Sort 3

Sort 3 defines the following records:

o MOD_FUNC	Module function.
o VENDOR	Module Producer.
o INTFC	Interface to the module population.
o COMP_INTOP	Is the bus interface compliant to the interoperability specifications underway for Pave Pillar?

3.1 Observations

Some VHSIC 1750A Computer vendors, including Westinghouse and Texas Instruments, are utilizing bus standards as defined by the Interoperability specifications. Proliferation of non-standard buses, however, is obvious from this sort. Several module types have IEEE-488 access. Several vendors indicated that high speed data bus (HSDB) modules will be standardized around specifications under development for a fiber optic bus.

4.0 Standard Electronic Module (SEM) - Sort 4/4A

Sort 4 defines the following records:

o MOD_FUNC	Module function.
o VENDOR	Module Producer.
o MOD_NAME	Program specific module [illegible]

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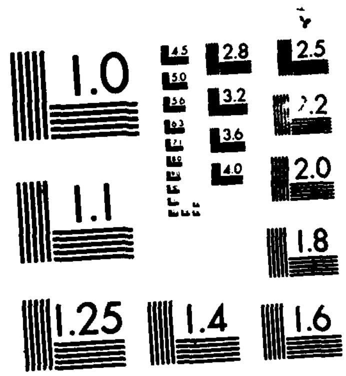

MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

- o SEM_COMPAT Is the module compatible to the existing SEM military standards (1389)?
- o HEGT module height.
- o WDTH module width.
- o LNTH module length.

Sort 4A defines the following records:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o MOD_NAME Program specific module name
- o SEM_COMPAT Is the module compatible to the existing SEM military standards (1389)?
- o SEM_SIZ SEM size (ie., A - E) per Mil-Std-1389
- o CONN_TYP Connector type, pin count

4.1 Observations

The extreme variation in module dimensions indicates that SEM standardization is incomplete or being ignored. Connector standardization towards the low insertion force (LIF) Malco or Teradyne is occurring. Standardization around the 304 pin connector is probable based on vendor follow-up interviews.

5.0 Autonomous Module Maintenance Processor/Time Stress Measurement Devices (TSMDs) - Sort 5

Sort 5 defines the following records:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o MOD_NAME Program specific module name
- o OPROCBF Does the module have an on-board processor dedicated to autonomous module test.
- o STRES_MEAS Are TSMDs present on the modules?

5.1 Observation

Time stress measurement devices are not incorporated in present designs by any of the vendors surveyed.

6.0 Device Mounting on Advanced System Modules - Sort 6

Sort 6 defines the following records:

- MOD_FUNC Module function.
- VENDOR Module Producer.
- MOD_NAME Program specific module name.
- CHPMNTCH Chip mounting technique on module.

6.1 Observations

Leaded surface mounting techniques and leadless chip carrier (LCC) methods predominated. This sort suggests that packaging standardization is not intended for the next generation of modules.

7.0 Device Packaging Details - Sort 7

Sort 7 defines the following records:

- MOD_FUNC Module function.
- VENDOR Module Producer.
- MOD_NAME Program specific module name.
- DVPKTCH1/2 Device packaging technical narrative

7.1 Observations

Detailed narratives from advanced system vendors indicates different mounting strategies from each company.

8.0 Technology Classification - Sort 8

Sort 8 defines the following records:

- MOD_FUNC Module function.
- VENDOR Module Producer.
- MOD_NAME Program specific module name.
- TCH_CLAS Technology classification

9.0 Module Functional Characteristics - Sort 9

Sort 9 defines the following records:

- MOD_FUNC Module function.
- VENDOR Module Producer.
- CHARACT Module characteristics narrative

9.1 Observations

This sort defines projected capabilities of each advanced module type.

10.0 Input Voltage/Power Dissipation Requirements - Sort 10

Sort 10 defines the following records:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o MOD_NAME Program specific module name.
- o VOLT_REQ1 Input voltage requirement
- o VOLT_REQ2 Input voltage requirement
- o VOLT_REQ3 Input voltage requirement
- o COOL_REQ Power dissipation in watts

10.1 Observations

When compared with sort 4, it is clear that development of a common module suite for advanced system architectures is not occurring. Standardization requires form, fit, and function transparency and pin-out commonality. Input voltage requirements vary from vendor to vendor which precludes interoperability through a standard backplane. The standard airborne transport rack (ATR) concept relies on system reconfiguration through a common backplane.

Power dissipation varied significantly with module function. Several power dissipation requirements appear difficult to meet with the conduction cooling mechanism of the Standard Electronic Module (SEM).

11.0 Module Technology (VHSIC phase I) by Module Function - Sort 11

Sort 11 defines the following records:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o SET_TCHN Technology incorporated in module.
- o TCH_CLAS Technology description
- o CHP_FUNC Chip function

11.1 Observations

This sort defines technologies incorporated by module function. A primary purposes of this sort was to discern standardization of bus interface units (BIUs) and module 1750A processors. Data is insufficient to draw conclusions about chip set technologies used for micro-processors and bus interfaces. VHSIC phase I specifications provided through DoD sponsored workshops, were significantly more accurate than this survey and, in several cases, showed conflicting information from inputs received by the questionnaire.

12.0 Module Technology (VHSIC phase II) by Module Function - Sort 12

Sort 12 defines the following records:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o SET_TCHN Technology incorporated in module.
- o TCH_CLAS Technology description
- o CHP_FUNC Chip function

12.1 Observations

Except for the IBM CBIU which incorporates 1.0 micron technology and the Honeywell input, the remaining data appears to be future projections for use of sub-micron VHSIC. Specification analyses and follow-up interviews have determined that hardware designed for the next generation of military avionics involves the use of phase I VHSIC.

13.0 Module Technology (VLSI) by Module Function - Sort 13/13A

Sort 13 defines the following records:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o SET_TCHN Technology incorporated in module.
- o TCH_CLAS Technology description
- o CHP_FUNC Chip function

13A is a sort on all technologies per module function and vendor. The following records include:

- o MOD_FUNC Module function.
- o VENDOR Module Producer.
- o SET_TCHN Technology incorporated in module.
- o TCH_CLAS Technology description
- o CHP_FUNC Chip function

13.1 Observations

Very little information was derived from this sort. Follow-up interviews indicated that "glue chips" would be a substantial part of next generation avionics.

TESTABILITY/ON-MODULE BIT PROCESSOR - SORT 1

MOD_FUNC	VENDOR	TEST_SCHM	OCLK_MOD	OPROCOP	OPROCBF
1553B	WESTINGHOUSE	BOUNDARY SCAN FITS	N	Y	N
1750	IBM				
		LSSD	Y	Y	Y
		SIGNATURE ANALYSIS	N	Y	Y
1750A	TEXAS INSTRUMENTS	BIST	N	Y	Y
1750A GP	WESTINGHOUSE	BOUNDARY SCAN FITS	Y	Y	Y
BULK MEMORY MODULE	WESTINGHOUSE	BOUNDARY SCAN FITS	N		
COM	TEXAS INSTRUMENTS	BIST	N	Y	Y
DATA NETWORK	IBM	BOUNDARY SCAN	N	N	N
DOPPLER FILTER, BUFFER	WESTINGHOUSE				
		PARITY			
		PSEUDO RANDOM TPG	N	N	N
		SERIAL SCAN			
		SIGNATURE ANALYSIS			
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE				
		PARITY			
		PSEUDO RANDOM TPG	N	N	N
		SERIAL SCAN			
		SIGNATURE ANALYSIS	N	N	N
FLOATING POINT PROCESSOR	IBM				
		BOUNDARY SCAN	N	N	N
		SIGNATURE ANALYSIS	N	Y	N
GLOBAL MEMORY	IBM				
		BOUNDARY SCAN	N	N	N
		SIGNATURE ANALYSIS	N		
HIGH SPEED COM	TEXAS INSTRUMENTS	BIST	N	Y	Y
HIGH SPEED DATA BUS	WESTINGHOUSE	BOUNDARY SCAN FITS	N	Y	N
HIGH SPEED E-O SIG PROC	HONEYWELL				
		SERIAL SCAN	N		
		SIGNATURE ANALYSIS	N	Y	Y
I/O TERMINATOR	IBM		N	N	N
INPUT/OUTPUT	TEXAS INSTRUMENTS	BIST	N	Y	Y
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE				
PI BUS TERMINATOR	IBM		N	N	N
POWER SUPPLIES	TEXAS INSTRUMENTS				
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE				
		BOUNDARY SCAN SET			
		SERIAL SCAN SET	N	Y	N
PULSE COMPRESSION/FFT	TRW				
		BIST	N	Y	Y
		SIGNATURE ANALYSIS	N	Y	
RANGE COMPRESSION, BGC	WESTINGHOUSE				
		PARITY			
		PSEUDO RANDOM TPG	N	N	N
		SERIAL SCAN			
		SIGNATURE ANALYSIS			
RANGE COMPRESSION BUFFER	WESTINGHOUSE				
		PARITY			
		PSEUDO RANDOM TPG	N	N	N
		SERIAL SCAN			
		SIGNATURE ANALYSIS			
SENSOR INTERFACE	IBM	BOUNDARY SCAN	N	N	N
TIMING AND CONTROL	TEXAS INSTRUMENTS	BIST	N	Y	Y
TIMING/CONTROL	IBM		Y	N	N

TESTABILITY/ON-MODULE BIT PROCESSOR - SORT 1

MOD_FUNC	VENDOR	TEST_SCHM	OCLK_MOD	OPROCOP	OPROCBF
USER CONSOLE INTERFACE	IBM		N	Y	N
VHSIC 1750A PROC	WR ALC	TBD	N	Y	Y

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AUTONOMOUS MODULE MAINTENANCE PROCESSOR - SORT 2

MOD FUNC	VENDOR	OPROCBF	OPROCBFCR
1553B	WESTINGHOUSE	N	
1750	IBM		
		Y	1750A INSTRUCTION SET
		Y	1750A ISA
1750A	TEXAS INSTRUMENTS	Y	4 WIRE SERIAL MAINTENANCE BUS
1750A GP	WESTINGHOUSE	Y	COMM 1750A PROC IN MMP WITH T/M BUS INTF
BULK MEMORY MODULE	WESTINGHOUSE		
COM	TEXAS INSTRUMENTS	Y	HAS SYS MAINTENANCE BUS, 4 WIRE SERIAL
DATA NETWORK	IBM	N	
DOPPLER FILTER, BUFFER	WESTINGHOUSE		
		N	NA
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE		
		N	NA
		N	NA
FLOATING POINT PROCESSOR	IBM		
		N	NA
		N	
GLOBAL MEMORY	IBM		
		N	FAULT HISTORY STORE DEVICE ON BOARD
HIGH SPEED COM	TEXAS INSTRUMENTS	Y	4 WIRE SERIAL SYS MAINTENANCE BUS
HIGH SPEED DATA BUS	WESTINGHOUSE	N	
HIGH SPEED E-O SIG PROC	HONEYWELL		
		Y	ADA, IEEE-488, PARALLEL ARCH, ETM/TM
I/O TERMINATOR	IBM	N	NA
INPUT/OUTPUT	TEXAS INSTRUMENTS	Y	4 WIRE T/M BUS ACCESS
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE		
PI BUS TERMINATOR	IBM	N	
POWER SUPPLIES	TEXAS INSTRUMENTS		
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE		
		N	NA
PULSE COMPRESSION/FFT	TRW		
		Y	EVERY SUPERCHIP HAS 16 BIT MAINT PROC
RANGE COMPRESSION, BGC	WESTINGHOUSE		
		N	NA
RANGE COMPRESSION, BUFFER	WESTINGHOUSE		
		N	NA
SENSOR INTERFACE	IBM	N	FAULT HISTORY STORE CHIP ON BOARD
TIMING AND CONTROL	TEXAS INSTRUMENTS	Y	4 WIRE SERIAL MAINT BUS ACCESS
TIMING/CONTROL	IBM	N	

AUTONOMOUS MODULE MAINTENANCE PROCESSOR - SORT 2

MOD_FUNC	VENDOR	OPROCBF	OPROCBFCR
USER CONSOLE INTERFACE	IBM	N	
VHSIC 1750A PROC	WR-ALC	Y	ON MODULE PROC FOR BIT - SOME VENDORS

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AUTONOMOUS MODULE MAINTENANCE PROCESSOR - SORT 2A

MOD_FUNC	VENDOR	OPROCBF	INTFC
1553B	WESTINGHOUSE	N	TEST/MAINTENANCE BUS
1750	IBM		EXTENDED T/M BUS
		Y	TEST/MAINTENANCE BUS
		Y	
1750A	TEXAS INSTRUMENTS	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
1750A GP	WESTINGHOUSE	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
BULK MEMORY MODULE	WESTINGHOUSE		EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
COM	TEXAS INSTRUMENTS	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
DATA NETWORK	IBM	N	
DOPPLER FILTER, BUFFER	WESTINGHOUSE		
		N	
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE		
		N	
		N	
FLOATING POINT PROCESSOR	IBM		
		N	
		N	
GLOBAL MEMORY	IBM		
		N	
HIGH SPEED COM	TEXAS INSTRUMENTS	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
HIGH SPEED DATA BUS	WESTINGHOUSE	N	TEST/MAINTENANCE BUS
HIGH SPEED E-O SIG PROC	HONEYWELL		EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
		Y	
I/O TERMINATOR	IBM	N	TEST/MAINTENANCE BUS
INPUT/OUTPUT	TEXAS INSTRUMENTS	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE		
PI BUS TERMINATOR	IBM	N	TEST/MAINTENANCE BUS
POWER SUPPLIES	TEXAS INSTRUMENTS		
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE		EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
		N	
PULSE COMPRESSION/FFT	TRW		TEST/MAINTENANCE BUS
		Y	
RANGE COMPRESSION, BGC	WESTINGHOUSE		
		N	
RANGE COMPRESSION BUFFER	WESTINGHOUSE		

AUTONOMOUS MODULE MAINTENANCE PROCESSOR - SORT 2A

MOD FUNC	VENDOR	OPROCBF	INTFC
RANGE COMPRESSION, BUFFER	WESTINGHOUSE	N	
SENSOR INTERFACE	IBM	N	
TIMING AND CONTROL	TEXAS INSTRUMENTS	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS
TIMING/CONTROL	IBM	N	TEST/MAINTENANCE BUS
USER CONSOLE INTERFACE	IBM	N	TEST/MAINTENANCE BUS
VHSIC 1750A PROC	WR-ALC	Y	EXTENDED T/M BUS
			TEST/MAINTENANCE BUS

ON-MODULE BIT PROCESSOR NARRATIVE SORT 2B

MOD_FUNC	VENDOR	OPROCBF	OPROCBFCR
1553B	WESTINGHOUSE	N	
1750	IBM		
		Y	1750A INSTRUCTION SET
		Y	1750A ISA
1750A	TEXAS INSTRUMENTS	Y	4 WIRE SERIAL MAINTENANCE BUS
1750A GP	WESTINGHOUSE	Y	COMM 1750A PROC IN MHP WITH T/M BUS INTF
BULK MEMORY MODULE	WESTINGHOUSE		
COM	TEXAS INSTRUMENTS	Y	HAS SYS MAINTENANCE BUS, 4 WIRE SERIAL
DATA NETWORK	IBM	N	
DOPPLER FILTER, BUFFER	WESTINGHOUSE		
		N	NA
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE		
		N	NA
		N	NA
FLOATING POINT PROCESSOR	IBM		
		N	NA
		N	
GLOBAL MEMORY	IBM		
		N	FAULT HISTORY STORE DEVICE ON BOARD
HIGH SPEED COM	TEXAS INSTRUMENTS	Y	4 WIRE SERIAL SYS MAINTENANCE BUS
HIGH SPEED DATA BUS	WESTINGHOUSE	N	
HIGH SPEED E-O SIG PROC	HONEYWELL		
		Y	ADA, IEEE-488, PARALLEL ARCH, ETM/TM
I/O TERMINATOR	IBM	N	NA
INPUT/OUTPUT	TEXAS INSTRUMENTS	Y	4 WIRE T/M BUS ACCESS
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE		
PI BUS TERMINATOR	IBM	N	
POWER SUPPLIES	TEXAS INSTRUMENTS		
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE		
		N	NA
PULSE COMPRESSION/FFT	TRW		
		Y	EVERY SUPERCHIP HAS 16 BIT MAINT PROC
RANGE COMPRESSION BGC	WESTINGHOUSE		
		N	NA
RANGE COMPRESSION, BUFFER	WESTINGHOUSE		
		N	NA
SENSOR INTERFACE	IBM	N	FAULT HISTORY STORE CHIP ON BOARD
TIMING AND CONTROL	TEXAS INSTRUMENTS	Y	4 WIRE SERIAL MAINT BUS ACCESS
TIMING/CONTROL	IBM	N	

ON MODULE BIT PROCESSOR NARRATIVE SORT 2B

MOD_FUNC	VENDOR	OPROCBF	OPROCBFCR
USER CONSOLE INTERFACE	IBM	N	
VHSIC 1750A PROC	WR ALC	Y	ON MODULE PROC FOR BIT - SOME VENDORS

BUS INTERFACE STANDARDIZATION-SORT 3

MOD FUNC	VENDOR	INTFC	COMP INTOP
1553B	WESTINGHOUSE	PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
1750	IBM	ELEMENT CONTROL BUS	N
		ELEMENT MAINTENANCE BUS	N
		EXTENDED T/M BUS	Y
		PARALLEL INTERFACE BUS	Y
		SYSTEM BREAKPOINT LINE	N
		SYSTEM RESET LINE	N
		TEST/MAINTENANCE BUS	Y
1750A	TEXAS INSTRUMENTS	EXTENDED T/M BUS	Y
		FIBER OPTIC HSDB	Y
		IEEE-488 BUS	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
1750A GP	WESTINGHOUSE	EXTENDED T/M BUS	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
BULK MEMORY MODULE	WESTINGHOUSE	EXTENDED T/M BUS	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
COM	TEXAS INSTRUMENTS	EXTENDED T/M BUS	Y
		FIBER OPTIC HSDB	Y
		IEEE-488	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
DATA NETWORK	IBM	DATA NETWORK BUS	N
		ELEMENT MAINTENANCE BUS	N
DOPPLER FILTER, BUFFER	WESTINGHOUSE	WEC VHSIC PSP FITS BUS	N
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE	VPSP FITS BUS	N
		VPSP SUB BUS	N
FLOATING POINT PROCESSOR	IBM	DATA NETWORK BUS	N
		ELEMENT CONTROL BUS	N
		ELEMENT MAINTENANCE BUS	N
GLOBAL MEMORY	IBM	DATA NETWORK BUS	N
		ELEMENT CONTROL BUS	N
		ELEMENT MAINTENANCE BUS	N
HIGH SPEED COM	TEXAS INSTRUMENTS	EXTENDED T/M BUS	Y
		FIBER OPTIC HSDB	Y
		IEEE 488	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
HIGH SPEED DATA BUS	WESTINGHOUSE	FIBER OPTIC HSDB	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
HIGH SPEED E O SIG PROC	HONEYWELL	EXTENDED T/M BUS	Y
		FIBER OPTIC HSDB	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
I/O TERMINATOR	IBM	1553B	Y
		BREAKPOINT	N
		IEEE-488	Y
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
INPUT/OUTPUT	TEXAS INSTRUMENTS	EXTENDED T/M BUS	Y

BUS INTERFACE STANDARDIZATION SORT 3

MOD FUNC	VENDOR	INTFC	COMP INTOP
INPUT/OUTPUT	TEXAS INSTRUMENTS	FIBER OPTIC HSDB	Y
		IEEE 488	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
PI BUS TERMINATOR	IBM	1553B	Y
		IEEE 488	Y
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE	EXTENDED T/M BUS	N
		PARALLEL INTERFACE BUS	N
		TEST/MAINTENANCE BUS	N
PULSE COMPRESSION/FFT	TRW	PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
RANGE COMPRESSION, BGC	WESTINGHOUSE	VPSP FITS BUS	N
RANGE COMPRESSION, BUFFER	WESTINGHOUSE	VPSP FITS BUS	N
		VPSP SUB BUS	N
SENSOR INTERFACE	IBM	DATA NETWORK BUS	N
		ELEMENT CONTROL BUS	N
		ELEMENT MAINTENANCE BUS	N
		SENSOR/VIDEO/FUSION BUS	N
TIMING AND CONTROL	TEXAS INSTRUMENTS	EXTENDED T/M BUS	Y
		FIBER OPTIC HSDB	Y
		IEEE 488	N
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y
TIMING/CONTROL	IBM	ELEMENT MAINTENANCE BUS	N
		TEST/MAINTENANCE BUS	Y
USER CONSOLE INTERFACE	IBM	PARALLEL INTERFACE BUS	Y
		SYSTEM BREAKPOINT	N
		TEST/MAINTENANCE BUS	Y
VHSIC 1750A PROC	WR ALC	1553B	Y
		EXTENDED T/M BUS	Y
		FIBER OPTIC HSDB	Y
		PARALLEL INTERFACE BUS	Y
		TEST/MAINTENANCE BUS	Y

STANDARD ELECTRONIC MODULE (SEM) SORT 4

MOD FUNC	VENDOR	MOD NAME	SEM COMPAT	HEGHT	WDTH	LNTH
1553B	WESTINGHOUSE	1553B INTERFACE MODULE	Y	5 44	0 58	6 41
1750	IBM					
		ELEMENT SUPERVISOR UNIT (ESU)	N	1 0	6 0	15 0
1750A	TEXAS INSTRUMENTS	V1750A	Y	6 7	5 9	0 5
1750A GP	WESTINGHOUSE					
		VHSIC 1750A CPU	Y			
BULK MEMORY MODULE	WESTINGHOUSE	BULK MEMORY MODULE	Y	5 44	0 58	6 41
CON	TEXAS INSTRUMENTS	1553B	Y	5 9	0 5	6 7
DATA NETWORK	IBM	DATA NETWORK ELEMENT MODULE	Y	6 40	0 6	5 88
DOPPLER FILTER, BUFFER	WESTINGHOUSE					
		DOPPLER FFT	N	12 2	11 5	
DOPPLER WEIGHT BUFFER	WESTINGHOUSE					
		INPUT BUFFER	N	12 2		11 5
FLOATING POINT PROCESSOR	IBM	FPPE	Y			
GLOBAL MEMORY	IBM	GLOBAL MEMORY MODULE	Y			
HIGH SPEED CON	TEXAS INSTRUMENTS	HSDB	Y	5 9	0 5	6 7
HIGH SPEED DATA BUS	WESTINGHOUSE	HSDB	Y	5 44	0 58	6 41
HIGH SPEED E O SIG PROC	HONEYWELL					
		E-O SIGNAL PROCESSOR	Y			
I/O TERMINATOR	IBM	I/O TERMINATOR MODULE	Y	6 40	0 6	5 88
INPUT/OUTPUT	TEXAS INSTRUMENTS	DISCRETE I/O	Y	5 9	0 5	6 7
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE	LOW VOLTAGE POWER SUPPLY	Y	5 44	0 58	6 41
PI BUS TERMINATOR	IBM	PI BUS TERMINATOR MODULE	Y	6 40	0 6	5 88
POWER SUPPLIES	TEXAS INSTRUMENTS	POWER SUPPLIES	Y	5 9	0 5	6 7
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE					
		SIGNAL PROCESSING MODULE	N	5 75	0 50	7 80
PULSE COMPRESSION/FFT	TRW					
		VHSIC PHASE 2 DEMO BRASSBOARD				
RANGE COMPRESSION BGC	WESTINGHOUSE					
		RANGE FFT	N	12 2		11 5
RANGE COMPRESSION BUFFER	WESTINGHOUSE					
		RANGE INVERSE FFT	N	12 2		11 5
SENSOR INTERFACE	IBM	SENSOR INTERFACE MODULE	Y	6 40	0 6	5 88
TIMING AND CONTROL	TEXAS INSTRUMENTS	TCG	Y	5 9	0 5	6 7
TIMING CONTROL	IBM	TIMING/CONTROL GENERATOR MODULE	Y	6 40	0 6	5 88
USER CONSOLE INTERFACE	IBM	USER CONSOLE INTERFACE MODULE	Y	6 40	0 6	5 88
VHSIC 1750A PROC	WR ALC					
		F 15 CC	Y			

STANDARD ELECTRONIC MODULE/CONNECTOR TYPE SORT 4A

MOD FUNC	VENDOR	MOD NAME	SEM COMPAT	SEM SIZE	CONN TYPE
1553B	WESTINGHOUSE	1553B INTERFACE MODULE	Y	E	250
1750	IBM	ELEMENT SUPERVISOR UNIT (ESU)	N		304 FIN
1750A	TEXAS INSTRUMENTS	V1750A	Y	E	250/310
1750A GP	WESTINGHOUSE	VHSIC 1750A CPU	Y	E	250 FIN
BULK MEMORY MODULE	WESTINGHOUSE	BULK MEMORY MODULE	Y	E	250
COM	TEXAS INSTRUMENTS	1553B	Y	E	250/304
DATA NETWORK	IBM	DATA NETWORK ELEMENT MODULE	Y	E	304
DOPPLER FILTER BUFFER	WESTINGHOUSE	DOPPLER FFT	N		
DOPPLER WEIGHT BUFFER	WESTINGHOUSE	INPUT BUFFER	N		
FLOATING POINT PROCESSOR	IBM	FPPE	Y		
GLOBAL MEMORY	IBM	GLOBAL MEMORY MODULE	Y		
HIGH SPEED COM	TEXAS INSTRUMENTS	HSDB	Y	E	250/304
HIGH SPEED DATA BUS	WESTINGHOUSE	HSDB	Y	E	250
HIGH SPEED E O SIG PROC	HONEYWELL	E O SIGNAL PROCESSOR	Y	E	
I/O TERMINATOR	IBM	I/O TERMINATOR MODULE	Y	E	304
INPUT/OUTPUT	TEXAS INSTRUMENTS	DISCRETE I/O	Y	E	250/304
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE	LOW VOLTAGE POWER SUPPLY	Y	E	250
PI BUS TERMINATOR	IBM	PI BUS TERMINATOR MODULE	Y	E	304
POWER SUPPLIES	TEXAS INSTRUMENTS	POWER SUPPLIES	Y	E	250
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE	SIGNAL PROCESSING MODULE	N		280 FIN
PULSE COMPRESSION/FFT	TRW	VHSIC PHASE 2 DEMO BRASSBOARD			
RANGE COMPRESSION BGC	WESTINGHOUSE	RANGE FFT	N		
RANGE COMPRESSION BUFFER	WESTINGHOUSE	RANGE INVERSE FFT	N		
SENSOR INTERFACE	IBM	SENSOR INTERFACE MODULE	Y	E	304
TIMING AND CONTROL	TEXAS INSTRUMENTS	TCG	Y	E	250/304
TIMING/CONTROL	IBM	TIMING/CONTROL GENERATOR MODULE	Y	E	304
USER CONSOLE INTERFACE	IBM	USER CONSOLE INTERFACE MODULE	Y	E	304
VHSIC 1750A PROC	MR ALC	F 15 CC	Y	E	WEC TRW

AUTONOMOUS MODULE PROCESSOR/TIME STRESS MEASUREMENT DEVICES SORT 5

MOD FUNC	VENDOR	MOD NAME	UPROCBF	STMI MEAS
1553B	WESTINGHOUSE	1553B INTERFACE MODULE	N	N
1750	IBM			
		ELEMENT SUPERVISOR UNIT (ESU)	Y	N
			Y	
1750A	TEXAS INSTRUMENTS	V1750A	Y	N
1750A GP	WESTINGHOUSE		Y	
		VHSIC 1750A CPU		N
BULK MEMORY MODULE	WESTINGHOUSE	BULK MEMORY MODULE		N
COM	TEXAS INSTRUMENTS	1553B	Y	N
DATA NETWORK	IBM	DATA NETWORK ELEMENT MODULE	N	N
DOPPLER FILTER BUFFER	WESTINGHOUSE			
		DOPPLER FFT		N
			N	
DOPPLER WEIGHT BUFFER	WESTINGHOUSE			
		INPUT BUFFER		N
			N	
			N	
FLOATING POINT PROCESSOR	IBM	FPPE		N
			N	
			N	
GLOBAL MEMORY	IBM	GLOBAL MEMORY MODULE		N
			N	
HIGH SPEED COM	TEXAS INSTRUMENTS	HSDB	Y	N
HIGH SPEED DATA BUS	WESTINGHOUSE	HSDB	N	N
HIGH SPEED E O SIG PROC	HONEYWELL			
		E O SIGNAL PROCESSOR		N
			Y	
I/O TERMINATOR	IBM	I/O TERMINATOR MODULE	N	N
INPUT/OUTPUT	TEXAS INSTRUMENTS	DISCRETE I/O	Y	N
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE	LOW VOLTAGE POWER SUPPLY		N
PI BUS TERMINATOR	IBM	PI BUS TERMINATOR MODULE	N	N
POWER SUPPLIES	TEXAS INSTRUMENTS	POWER SUPPLIES		N
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE			
		SIGNAL PROCESSING MODULE		N
			N	
PULSE COMPRESSION FFT	TRW			
		VHSIC PHASE 2 DEMO BRASSBOARD	Y	
RANGE COMPRESSION BUF	WESTINGHOUSE			
		RANGE FFT		N
			N	
RANGE COMPRESSION BUFFER	WESTINGHOUSE			
		RANGE INVERSE FFT		N
			N	
SENSOR INTERFACE	HM	SENSOR INTERFACE MODULE	N	N
TIMING AND CONTROL	TEXAS INSTRUMENTS	T&C	Y	N

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AUTONOMOUS MODULE PROCESSOR TIME STRESS MEASUREMENT DEVICES SORT 5

MOD FUNC	VENDOR	MOD NAME	OPROCBF	STRES MEA
TIMING/CONTROL	IBM	TIMING CONTROL GENERATOR MODULE	N	N
USER CONSOLA INTERFACE	IBM	USER CONSOLE INTERFACE MODULE	N	N
VHSIC 1750A PROC	WR ALC	F 15 CC	Y	Y

DEVICE MOUNTING ON ADVANCED SYSTEM MODULES SORT 6

MOD FUNC / MOD NAME	VENDOR	CHPMNTCH
1553B	WESTINGHOUSE	
1553B INTERFACE MODULE		SURFACE MOUNT
1750	IBM	
ELEMENT SUPERVISOR UNIT (ESU)		SURFACE MOUNT
1750A	TEXAS INSTRUMENTS	
V1750A		LEADLESS CHIP CARRIERS
1750A GP	WESTINGHOUSE	
VHSIC 1750A CPU		SURFACE MOUNT
BULK MEMORY MODULE	WESTINGHOUSE	
BULK MEMORY MODULE		SURFACE MOUNT
COM	TEXAS INSTRUMENTS	
1553B		LEADLESS CHIP CARRIERS SURFACE MOUNT
DATA NETWORK	IBM	
DATA NETWORK ELEMENT MODULE		LCC
DOPPLER FILTER BUFFER	WESTINGHOUSE	
DOPPLER FFT		
DOPPLER WEIGHT BUFFER	WESTINGHOUSE	
INPUT BUFFER		
FLOATING POINT PROCESSOR	IBM	
FPPE		LCC
GLOBAL MEMORY	IBM	
GLOBAL MEMORY MODULE		LCC
HIGH SPEED COM	TEXAS INSTRUMENTS	
HSDB		LEADLESS CHIP CARRIERS, SURFACE MOUNT
HIGH SPEED DATA BUS	WESTINGHOUSE	
HSDB		SURFACE MOUNT
HIGH SPEED I O SIG PROC	HONEYWELL	
I O SIGNAL PROCESSOR		
I O TERMINATOR	IBM	
I O TERMINATOR MODULE		LCC
INPUT OUTPUT	TEXAS INSTRUMENTS	
DISCRETE I O		LEADLESS CHIP CARRIERS
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE	
LOW VOLTAGE POWER SUPPLY		
PI BUS TERMINATOR	IBM	
PI BUS TERMINATOR MODULE		LCC
POWER SUPPLIES	TEXAS INSTRUMENTS	
POWER SUPPLIES		
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE	
SIGNAL PROCESSING MODULE		SURFACE MOUNT
PULSE COMPRESSION/FFT	TRW	
VHSIC PHASE 1 DEMO BRASSBOARD		
RANGE COMPRESSION BUF	WESTINGHOUSE	
RANGE FFT		

DEVICE MOUNTING ON ADVANCED SYSTEM MODULES SORT 6

MOD FUNC / MOD NAME	VENDOR	CHPMNTCH
RANGE COMPRESSION BUFFER	WESTINGHOUSE	
RANGE INVERSE FFT		
SENSOR INTERFACE	IBM	
SENSOR INTERFACE MODULE		LEADLESS CHIP CARRIERS
TIMING AND CONTROL	TEXAS INSTRUMENTS	
TCG		LEADLESS CHIP CARRIER, SURFACE MOUNT
TIMING/CONTROL	IBM	
TIMING/CONTROL GENERATOR MODULE		LCC
USER CONSOLE INTERFACE	IBM	
USER CONSOLE INTERFACE MODULE		LCC
VHSIC 1750A PROC	WR ALC	
F 15 CC		SURFACE MOUNTED

DEVICE PACKAGING DETAILS SORT 7

```
MOD FUNC                     VENDOR                    MOD NAME
--------                     ------                    --------
  DVPETCHI
  --------
1553B                        WESTINGHOUSE              1553B INTERFACE MODULE
  MMP. CHIP CARRIERS. FLAT PACKS
1750                         IBM

                                                       ELEMENT SUPERVISOR UNIT (ESU)
  LEADLESS CHIP CARRIERS (20,28,32,44 PAD). FLAT PACKS
1750A                        TEXAS INSTRUMENTS         V1750A
  CERAMIC DEVICES MOUNTED ON CERAMIC OR ADVANCED POLYMER
1750A GP                     WESTINGHOUSE

                                                       VHSIC 1750A CPU
  MMP. CHIP CARRIER. FLAT PACKS
BULK MEMORY MODULE           WESTINGHOUSE              BULK MEMORY MODULE
  MMPS. CHIP CARRIERS. FLATPACKS
COM                          TEXAS INSTRUMENTS         1553B
  CERAMIC DEVICES MOUNTED ON CERAMIC OR ADVANCED POLYMER
DATA NETWORK                 IBM                       DATA NETWORK ELEMENT MODULE

DOPPLER FILTER. BUFFER       WESTINGHOUSE

                                                       DOPPLER FFT
  DUAL IN LINE PACKAGING. PIN GRID ARRAYS
DOPPLER WEIGHT. BUFFER       WESTINGHOUSE

                                                       INPUT BUFFER
  DUAL IN LINE PACKAGES  PIN GRID ARRAYS
FLOATING POINT PROCESSOR     IBM                       FPPE
  MULTICHIP CARRIERS
GLOBAL MEMORY                IBM                       GLOBAL MEMORY MODULE
  MULTICHIP CARRIERS
HIGH SPEED COM               TEXAS INSTRUMENTS         HSDB
  CERAMIC DEVICES MOUNTED ON CERAMIC OR ADVANCED POLYMER
HIGH SPEED DATA BUS          WESTINGHOUSE              HSDB
  WIRE OR FIBER INTFC  MMPS. CHIP CARRIERS. FLAT PACKS
HIGH SPEED E O SIG PROC      HONEYWELL

                                                       E O SIGNAL PROCESSOR
  LEADLESS CHIP CARRIERS. PIN GRID ARRAYS. MULTIPLE CHIP
I/O TERMINATOR               IBM                       I/O TERMINATOR MODULE

INPUT/OUTPUT                 TEXAS INSTRUMENTS         DISCRETE I/O
  CERAMIC DEVICES MOUNTED ON CERAMIC OR POLYMER ON METAL
LOW VOLTAGE POWER SUPPLY     WESTINGHOUSE              LOW VOLTAGE POWER SUPPLY

PI BUS TERMINATOR            IBM                       PI BUS TERMINATOR MODULE

POWER SUPPLIES               TEXAS INSTRUMENTS         POWER SUPPLIES

PROGRAMMABLE SIGNAL PROC     WESTINGHOUSE

                                                       SIGNAL PROCESSING MODULE
  124/28/16 PIN 20 20 50 MIL CENTER LEADED FLATPACKS
```

DEVICE PACKAGING DETAILS-SORT 7

MOD FUNC	VENDOR	MOD NAME
DVPKTCHI		
PULSE COMPRESSION/FFT	TRW	
		VHSIC PHASE 2 DEMO BRASSBOARD
RANGE COMPRESSION, BGC	WESTINGHOUSE	
		RANGE FFT
DUAL IN LINE PACKAGES, PIN GRID ARRAYS		
RANGE COMPRESSION, BUFFER	WESTINGHOUSE	
		RANGE INVERSE FFT
DUAL IN-LINE PACKAGING, PIN GRID ARRAYS		
SENSOR INTERFACE	IBM	SENSOR INTERFACE MODULE
HERMETICALLY SEALED LCC, JEDEC CARRIERS, MULTICHIP		
TIMING AND CONTROL	TEXAS INSTRUMENTS	TCG
CERAMIC DEVICES MOUNTED ON CERAMIC OR ADVANCED POLYMER		
TIMING/CONTROL	IBM	TIMING/CONTROL GENERATOR MODULE
DEVICES MOUNTED ON EXPOXY KEVLAR/FIBERGLASS BOARD.		
USER CONSOLE INTERFACE	IBM	USER CONSOLE INTERFACE MODULE
VHSIC 1750A PROC	WR-ALC	
		F 15 CC
TWO SIDED CIRCUIT BOARDS		

TECHNOLOGY CLASSIFICATION SORT 8

MOD FUNC / MOD NAME	VENDOR	TCH CLAS
1553B	WESTINGHOUSE	
1553B INTERFACE MODULE		
1750	IBM	
ELEMENT SUPERVISOR UNIT (ESU)		ECL GATE ARRAY WITH TTL OUTPUTS
		SEMI-CUSTOM GATE ARRAY. DRC AND ECBM ARE GATE ARRAYS
		SEMI-CUSTOM
		MSI - FAST
		SEMI-CUSTOM
		SEMI-CUSTOM
1750A	TEXAS INSTRUMENTS	
V1750A		
		STD
		ROM CONTROLLER
		CUSTOM
		STL, NMOS, CMOS
		20K GATE ARRAY
1750A GP	WESTINGHOUSE	
		SEMI-CUSTOM ASIC
VHSIC 1750A CPU		SEMI CUSTOM
		SEMI-CUSTOM
BULK MEMORY MODULE	WESTINGHOUSE	
BULK MEMORY MODULE		
COM	TEXAS INSTRUMENTS	
1553B		
		STL, NMOS, CMOS
DATA NETWORK	IBM	
DATA NETWORK ELEMENT MODULE		
DOPPLER FILTER, BUFFER	WESTINGHOUSE	
DOPPLER FFT		FAIRCHILD FAST
		STANDARD
		10K CMOS GATE ARRAY
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE	
INPUT BUFFER		FAIRCHILD FAST
		STANDARD
		10K CMOS GATE ARRAYS

TECHNOLOGY CLASSIFICATION SORT 8

MOD_FUNC / MOD NAME	VENDOR	TCH CLAS
FLOATING POINT PROCESSOR	IBM	
FPPE		
GLOBAL MEMORY	IBM	
GLOBAL MEMORY MODULE		
HIGH SPEED COM	TEXAS INSTRUMENTS	
HSDB		
		STL, NMOS, CMOS
HIGH SPEED DATA BUS	WESTINGHOUSE	
HSDB		
HIGH SPEED E-O SIG PROC	HONEYWELL	
E-O SIGNAL PROCESSOR		1.25 VHSIC LIKE CMOS GATE ARRAY
		BIPOLAR (ISL)(CML) CUSTOM; GATE ARRAYS
		BIPOLAR (CML), MIXED (CUSTOM, GATE ARRAY)
		CMOS RAM, BIPOLAR CUSTOM
I/O TERMINATOR	IBM	
I/O TERMINATOR MODULE		
INPUT/OUTPUT	TEXAS INSTRUMENTS	
DISCRETE I/O		
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE	
LOW VOLTAGE POWER SUPPLY		
PI BUS TERMINATOR	IBM	
PI BUS TERMINATOR MODULE		
POWER SUPPLIES	TEXAS INSTRUMENTS	
POWER SUPPLIES		
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE	
SIGNAL PROCESSING MODULE		PROGRAMMABLE READ ONLY MEMORY
		RESISTOR NETWORK
		BULK CMOS, 5V PWR SPLY, CMOS I/O
PULSE COMPRESSION/FFT	TRW	
VHSIC PHASE 2 DEMO BRASSBOARD		GEN PURPOSE
RANGE COMPRESSION, BGC	WESTINGHOUSE	

TECHNOLOGY CLASSIFICATION-SORT 8

MOD_FUNC / MOD_NAME	VENDOR	TCH_CLAS
RANGE COMPRESSION, BGC	WESTINGHOUSE	
RANGE FFT		FAIRCHILD FAST STANDARD
		10K CMOS GATE ARRAY
RANGE COMPRESSION, BUFFER	WESTINGHOUSE	
RANGE INVERSE FFT		FAIRCHILD FAST STANDARD 10K CMOS GATE ARRAY
SENSOR INTERFACE	IBM	
SENSOR INTERFACE MODULE		
TIMING AND CONTROL	TEXAS INSTRUMENTS	
TCG		
		20K GATE ARRAY
TIMING/CONTROL	IBM	
TIMING/CONTROL GENERATOR MODULE		
USER CONSOLE INTERFACE	IBM	
USER CONSOLE INTERFACE MODULE		
VHSIC 1750A PROC	WR-ALC	
F-15 CC		
		SOURCE SELECTION DEPENDENT

MODULE FUNCTIONAL CHARACTERISTICS-SORT 9

MOD_FUNC / MOD_NAME	VENDOR	CHARACT
1553B	WESTINGHOUSE	
1553B INTERFACE MODULE		DUAL REDUNDANT 1553 INTFC, 4 OPERATIONAL MODES. XIO CONTROL
1553B INTERFACE MODULE		
1750	IBM	
ELEMENT SUPERVISOR UNIT (ESU)		
ELEMENT SUPERVISOR UNIT (ESU)		256K PROGRAM STORE. 1750A INSTRUCTION SET. 0 8 MIPS
ELEMENT SUPERVISOR UNIT (ESU)		CONTROLS OPERATION OF FUNCTIONAL ELEMENT (FE), PROVIDES
ELEMENT SUPERVISOR UNIT (ESU)		MAINTENANCE SUPPORT FOR FUNCTIONAL ELEMENT GROUP (FEG). MTBF
ELEMENT SUPERVISOR UNIT (ESU)		44000 HRS. 12 5 MHZ DATA RATE
ELEMENT SUPERVISOR UNIT (ESU)		
1750A	TEXAS INSTRUMENTS	
V1750A		VHSIC 1750A CPU, 256K WORDS. 3 MIPS. SEM-E. ADA PROG.
V1750A		
1750A GP	WESTINGHOUSE	
VHSIC 1750A CPU		
VHSIC 1750A CPU		2 0 MIPS. 256K RAM JOVIAL, ADA, DUAL-PI BUS
VHSIC 1750A CPU		
VHSIC 1750A CPU		
BULK MEMORY MODULE	WESTINGHOUSE	
BULK MEMORY MODULE		2 MEGA WORDS VOLATILE MEMORY, SEM-E, 1 MEGABIT CONTROLLER
BULK MEMORY MODULE		OPERATES AT 1/3 TO 1/4 PI-BUS FREQ
COM	TEXAS INSTRUMENTS	
1553B		V1750A, 256K WORDS, 3 MIPS, SEM-E, DUAL PI-BUS, ADA
1553B		
DATA NETWORK	IBM	
DATA NETWORK ELEMENT MODULE		HIGH SPEED LOCAL AREA NETWORK BETWEEN FE'S, 300 M, 32 BIT
DATA NETWORK ELEMENT MODULE		WORDS/SEC
DATA NETWORK ELEMENT MODULE		
DOPPLER FILTER, BUFFER	WESTINGHOUSE	
DOPPLER FFT		
DOPPLER FFT		120 POINT FFT, 24 BIT, RPL/12 LANGUAGE, 800 MIPS, 32K X 52
DOPPLER FFT		RAM
DOPPLER FFT		
DOPPLER WEIGHT, BUFFER	WESTINGHOUSE	
INPUT BUFFER		
INPUT BUFFER		200 MIPS, 20 BITS, 32 X 20 RAM, RPL/12 LANGUAGE
INPUT BUFFER		
FLOATING POINT PROCESSOR	IBM	
FPPE		2 MODULE ASSEMBLIES ELECTRICALLY AND MECHANICALLY CONNECTED
FPPE		PROVIDES HIGH SPEED VECTOR AND SCALAR FLOATING POINT AND
FPPE		FIXED POINT PROCESSING, 25 MHZ OPS
FPPE		
GLOBAL MEMORY	IBM	
GLOBAL MEMORY MODULE		1 MEGAWORD MEMORY, 32 BIT STORAGE WITH COMPLEX ADDRESSING
GLOBAL MEMORY MODULE		FUNCTION. HIGH SPEED BULK STORAGE. 25 MHZ OPS. ERROR
GLOBAL MEMORY MODULE		DETECTION/CORRECTION
GLOBAL MEMORY MODULE		
HIGH SPEED COM	TEXAS INSTRUMENTS	
HSDB		V1750A, 256K WORDS, 3 MIP, SEM E, DUAL PI BUS, ADA

MODULE FUNCTIONAL CHARACTERISTICS-SORT 9

```
MOD_FUNC                   VENDOR
--------                   ------
  MOD_NAME                                  CHARACT
  --------                                  -------
HIGH SPEED COM             TEXAS INSTRUMENTS
  HSDB
HIGH SPEED DATA BUS        WESTINGHOUSE
  HSDB                                      BREADBOARD INCLUDES 1750A VLSI CONTROLLER, HSDB EN/DECODER
  HSDB
HIGH SPEED E-O SIG PROC    HONEYWELL

  E-O SIGNAL PROCESSOR
  E-O SIGNAL PROCESSOR                      800 MOPS, 33 PROCESSING ELEMENTS (PE) ARE CONFIGURED, BUT
  E-O SIGNAL PROCESSOR                      ONLY 32 ARE USED, 1 USED FOR FAULT TOLERANCE. SYS IS
  E-O SIGNAL PROCESSOR                      CONFIGURABLE DEPENDING ON WINDOW SIZE (PIXELS) AND COMPLEX
  E-O SIGNAL PROCESSOR                      ITY OF ALGORITHMS. EACH PE CAPABLE OF 20 MOPS. UNIT INTER-
  E-O SIGNAL PROCESSOR                      FACES WITH LOCAL BUS
  E-O SIGNAL PROCESSOR
I/O TERMINATOR             IBM
  I/O TERMINATOR MODULE                     500000 HR MTBF
INPUT/OUTPUT               TEXAS INSTRUMENTS
  DISCRETE I/O                              DUAL PI-BUS
  DISCRETE I/O
LOW VOLTAGE POWER SUPPLY   WESTINGHOUSE
  LOW VOLTAGE POWER SUPPLY                  SEM-E.
PI BUS TERMINATOR          IBM
  PI BUS TERMINATOR MODULE                  PI BUS TERMINATOR, 821000 MTBF
  PI BUS TERMINATOR MODULE
POWER SUPPLIES             TEXAS INSTRUMENTS
  POWER SUPPLIES                            SEM-E
  POWER SUPPLIES
PROGRAMMABLE SIGNAL PROC   WESTINGHOUSE

  SIGNAL PROCESSING MODULE
  SIGNAL PROCESSING MODULE                  20 MCOPS, 64K LOCAL MEMORY, 8K MICROCODE MEMORY, 2
  SIGNAL PROCESSING MODULE                  PARALLEL DATA I/O PORTS, ADA PROG
  SIGNAL PROCESSING MODULE
PULSE COMPRESSION/FFT      TRW

  VHSIC PHASE 2 DEMO BRASSBOARD
  VHSIC PHASE 2 DEMO BRASSBOARD             PREPROCESSING 13 BOPS, SIG PROC, 400 MFLOPS, MEMORY, 10
  VHSIC PHASE 2 DEMO BRASSBOARD             MBITS, ADA PROGAMMABLE, SEU PROTECTED, SINGLE PORT FAILURE
  VHSIC PHASE 2 DEMO BRASSBOARD             PROTECTED BUSES
  VHSIC PHASE 2 DEMO BRASSBOARD
RANGE COMPRESSION, BGC     WESTINGHOUSE

  RANGE FFT
  RANGE FFT                                 210 POINT FFT, 12 BIT, RPL 12 LANGUAGE, 1000 MIPS, 4K X 12
  RANGE FFT                                 RAM
  RANGE FFT
RANGE COMPRESSION BUFFER   WESTINGHOUSE

  RANGE INVERSE FFT
  RANGE INVERSE FFT                         210 POINT FFT, 12 BIT, RPL 12 LANGUAGE, 1000 MIPS, 4K X 16
  RANGE INVERSE FFT                         RAM
  RANGE INVERSE FFT
```

MODULE FUNCTIONAL CHARACTERISTICS SORT 9

```
MOD_FUNC                        VENDOR
--------                        ------
  MOD_NAME                                              CHARACT
  --------                                              -------
SENSOR INTERFACE                IBM
  SENSOR INTERFACE MODULE                               INTFC TO SENSORS, VIDEO, FUSION NETWORKS.  12.5 MHZ (400
  SENSOR INTERFACE MODULE                               MEGABITS/SEC) I/O.
  SENSOR INTERFACE MODULE
TIMING AND CONTROL              TEXAS INSTRUMENTS
  TCQ                                                   1750A, 256K WORD, 3 MIPS, SEM-E, ADA, DUAL PI BUS
  TCQ
TIMING/CONTROL                  IBM
  TIMING/CONTROL GENERATOR MODULE                       PROVIDES ALL CLOCKS FOR USER/CONSOLE INTFC MODULE.
  TIMING/CONTROL GENERATOR MODULE                       PROVIDES 25 MHZ, 12.5 MHZ, AND 6.25 MHZ CLOCKS
  TIMING/CONTROL GENERATOR MODULE
USER CONSOLE INTERFACE          IBM
  USER CONSOLE INTERFACE MODULE                         SERVES AS INTFC BETWEEN CONSOLE AND CSP
VHSIC 1750A PROC                WR-ALC

  F-15 CC
  F-15 CC                                               3-5 MIPS, 2 MEGAWORDS GLOBAL, 256K WORDS LOCAL. ADA JOVIAL J73
  F-15 CC                                               FAULT TOLERANT, SELF DIAGNOSTICS, TIME STRESS MEASUREMENT
  F-15 CC                                               DEVICES.  TWO-LEVEL MAINTENANCE CAPABLE
  F-15 CC
```

INPUT VOLTAGE/POWER DISSIPATION REQUIREMENTS SORT 10

MOD FUNC / MOD NAME	VENDOR	VOLT REQ1	VOLT REQ2	VOLT REQ3	COOL REQ
1553B	WESTINGHOUSE				
1553B INTERFACE MODULE		5.0			
1750	IBM				
ELEMENT SUPERVISOR UNIT (ESU)		5.0	1.0		82
1750A	TEXAS INSTRUMENTS				
V1750A		5.0	3.3	2.0	26.0
1750A GP	WESTINGHOUSE				
VHSIC 1750A CPU		5.0			
BULK MEMORY MODULE	WESTINGHOUSE				
BULK MEMORY MODULE		5.0			
COM	TEXAS INSTRUMENTS				
1553B		5.0	3.3	2.0	.6
DATA NETWORK	IBM				
DATA NETWORK ELEMENT MODULE		5.0			3.8
DOPPLER FILTER BUFFER	WESTINGHOUSE				
DOPPLER FFT		5.0	5.2		65
DOPPLER WEIGHT BUFFER	WESTINGHOUSE				
INPUT BUFFER		5.0	5.2		65
FLOATING POINT PROCESSOR	IBM				
FPPE		5.0			46.5
GLOBAL MEMORY	IBM				
GLOBAL MEMORY MODULE		5.0	1.0		24.4
HIGH SPEED COM	TEXAS INSTRUMENTS				
HSDB		5.0	3.3	2.0	.6
HIGH SPEED DATA BUS	WESTINGHOUSE				
HSDB		5.0			
HIGH SPEED E O SIG PROC	HONEYWELL				
E O SIGNAL PROCESSOR		TTL			100
I/O TERMINATOR	IBM				
I/O TERMINATOR MODULE		5.0	[illegible]		4
INPUT OUTPUT	TEXAS INSTRUMENTS				
DISCRETE I/O		[illegible]	[illegible]	[illegible]	[illegible]
LOW VOLTAGE POWER SUPPLY	WESTINGHOUSE				
LOW VOLTAGE POWER SUPPLY		[illegible]	[illegible]	.8	
FT BUS TERMINATOR	IBM				
FT BUS TERMINATOR MODULE		[illegible]			[illegible]
POWER SUPPLIES	TEXAS INSTRUMENTS				
POWER SUPPLIES					[illegible]
PROGRAMMABLE SIGNAL PROC	WESTINGHOUSE				
[illegible]		[illegible]			[illegible]
[illegible] FFT	TRW				
[illegible]					
RANGE [illegible]	[illegible]				
RANGE FFT					

PAGE

INPUT VOLTAGE POWER DISSIPATION REQUIREMENTS [illegible]

MOD FUNC	VENDOR				
MOD NAME		VOLT REQ1	VOLT REQ2	VOLT REQ3	[illegible] REQ
RANGE COMPRESSION BUFFER	WESTINGHOUSE				
RANGE INVERSE FFT		[illegible]	[illegible]		[illegible]
SENSOR INTERFACE	IBM				
SENSOR INTERFACE MODULE		5 [illegible]	[illegible]		[illegible]
TIMING AND CONTROL	TEXAS INSTRUMENTS				
TCG		[illegible]	[illegible]	[illegible]	[illegible]
TIMING CONTROL	IBM				
TIMING/CONTROL GENERATOR MODULE		[illegible]			[illegible]
USER CONSOLE INTERFACE	IBM				
USER CONSOLE INTERFACE MODULE		[illegible]	[illegible]		[illegible]
VHSIC 1750A PBIX	WR ALC				

[illegible]

MODULE TECHNOLOGIES SORT [illegible]

MOD FUNC	VENDOR	SAT TCHN	
TCH CLAS			CMP FUNC
1553B	WESTINGHOUSE	VHSIC 1	PI BUS DRIVERS
1750	IBM	VHSIC 1	1750A
1750A STL MBUS CMOS	TEXAS INSTRUMENTS	VHSIC 1	PU SRAM INTF
1750A GP SEMI CUSTOM	WESTINGHOUSE	VHSIC 1	PU PI BUS
BULK MEMORY MODULE	WESTINGHOUSE	VHSIC 1	PI BUS
[illegible] STL MBUS CMOS	TEXAS INSTRUMENTS	VHSIC 1	PU SRAM INTF
DOPPLER FILTER BUFFER 10K CMOS GATE ARRAY	WESTINGHOUSE	VHSIC 1	AU BIT FIT
DOPPLER WEIGHT BUFFER 10K CMOS GATE ARRAYS	WESTINGHOUSE	VHSIC 1	AU ASYNC INTF BIT FIT
GLOBAL MEMORY	IBM	VHSIC 1	GATE ARRAYS
HIGH SPEED [illegible] STL MBUS CMOS	TEXAS INSTRUMENTS	VHSIC 1	PU SRAM INTF
HIGH SPEED DATA BUS	WESTINGHOUSE	VHSIC 1	1750A PU PI BUS INTF
HIGH SPEED [illegible] SIG PROC BIPOLAR ISL [illegible] CUSTOM GATE ARRAYS	HONEYWELL	VHSIC 1	HIGH SPEED ARITH RAM [illegible]
INPUT OUTPUT	TEXAS INSTRUMENT	VHSIC 1	PU SRAM INTF
PROGRAMMABLE SIGNAL PROC BULK CMOS [illegible] SPLT [illegible]	WESTINGHOUSE	VHSIC [illegible]	
RANGE COMPRESSION [illegible] 10K CMOS GATE ARRAY	WESTINGHOUSE	VHSIC [illegible]	A BIT FIT
RANGE COMPRESSION BUFFER 10K CMOS GATE ARRAY	WESTINGHOUSE	VHSIC 1	AU ASYNC INTF BIT FIT
TIMING AND CONTROL	TEXAS INSTRUMENTS	VHSIC 1	PU SRAM INTF
VHSIC 1750A PROC SOURCE SELECTION DEPENDENT	[illegible]	VHSIC [illegible]	PU MEMORY

PAGE

MODULE TECHNOLOGIES SORT

MOD FUNC	VENDOR	SET TECH	
TCH CLAS			HF FUN
1750	TRW	VHSI[illegible]	
SEMI CUSTOM			BI[illegible]
1750A	TEXAS INSTRUMENTS	VHSI[illegible]	
20K GATE ARRAY			[illegible] BUS CONTROLLER
1750A GP	WESTINGHOUSE	VHSI[illegible]	
HIGH SPEED COM	TEXAS INSTRUMENTS	VHSI[illegible]	
			[illegible] BUS CONTROLLER
HIGH SPEED & [illegible] SIG PROC	HONEYWELL	VHSI[illegible]	
BIPOLAR (CML) [illegible] MIXED	CUSTOM GATE ARRAY		HIGH SPEED [illegible] INTF [illegible]
PULSE COMPRESSION FFT	TRW	VHSI[illegible]	
GEN PURPOSE			PREPROCESSING [illegible] MEMORY
TIMING AND CONTROL	TEXAS INSTRUMENTS	VHSI[illegible]	
[illegible] GATE ARRAY			[illegible] BUS CONTROLLER

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MODULE TECHNOLOGIES SORT 11

MOD FUNC	VENDOR	SET TCHN	HI FUNC
TCH CLAS			
1553B	WESTINGHOUSE	VLSI	
1750	IBM	VLSI	1750A CHIP SET
SEMI CUSTOM 1750A	TEXAS INSTRUMENTS	VLSI	DEMO CPU SAU PM X 1K STARTUP ROM
BULK MEMORY MODULE	WESTINGHOUSE	VLSI	DRAMC DRAM CONTROLLER
COM	TEXAS INSTRUMENTS	VLSI	
DATA NETWORK	IBM	VLSI	
GLOBAL MEMORY	IBM	VLSI	
HIGH SPEED COM	TEXAS INSTRUMENTS	VLSI	
HIGH SPEED DATA BUS	WESTINGHOUSE	VLSI	
HIGH SPEED & O SIG PROC	HONEYWELL	VLSI	
CMOS RAM BIPOLAR CUSTOM			16K RAM CMOS HIGH SPEED ARRAY PROC
I/O TERMINATOR	IBM	VLSI	
INPUT OUTPUT	TEXAS INSTRUMENTS	VLSI	
SENSOR INTERFACE	IBM	VLSI	
TIMING AND CONTROL	TEXAS INSTRUMENTS	VLSI	
VHSIC 1750A PROC	WR ALC	VLSI	GLUE CHIPS

APPENDIX F

FOCUS Data Base Software

PROCEDURE

Procedure for using the VHSIC data base.

A. ASSUMPTION:
FOCUS loaded on hard disk
User familiar with FOCUS.

B. PROCESS:
Enter into FOCUS

Example:
CD \FOCUS '<ENTER>'
FOCUS

Type
EX ATSM '<ENTER>'

C. OUTPUT:
For reports consult your FOCUS manual under TABLETALK. The name of the master file is 'ATS.MAS'.

D. MASTER FILE DESCRIPTION:
See Figure F-1.

E. COMMENTS:

This FOCUS procedure uses the Dialogue Manager (figure 2) to allow several modules to work in conjunction with each other. The Dialogue Manager stores the top two (2) keys in a file called 'VHS.DATA'. The Dialogue Manager then invokes a module called 'ATSL.FEX' that checks the status of the two keys. Then it invokes three (3) different modules that are screen modules which will allow the user to enter and/or update 'VHSIC/ATS VENDOR SURVEY data. The listings of these modules can be found in Figure F-2. After the screens are completed, the Dialogue Manager asks the user to press the '<F3>' function key or the '<ENTER>' key. The '<F3>' will return the user to the FOCUS operating system while the '<ENTER>' key will allow the user to enter two new keys and walk through the process again.

```
FILENAME=ATS SUFFIX=FOC $
SEGNAME=MOD_SEG SEGTYPE=S1 $
   FIELD=MOD_FUNC,        ALIAS=MF,       FORMAT=A25 $
SEGNAME=VENDSEG,PARENT=MOD_SEG SEGTYPE=S1 $
   FIELD=VENDOR,          ALIAS=VND,      FORMAT=A25 $
   FIELD=SLOG_0VT,        ALIAS=SL0V,     FORMAT=A4 $
   FIELD=SLOG_1VT,        ALIAS=SL1V,     FORMAT=A4 $
   FIELD=SLOG_0P,         ALIAS=SL0P      FORMAT=A4 $
   FIELD=SLOG_1P,         ALIAS=SL1P,     FORMAT=A4 $
   FIELD=SMIN_SNK,        ALIAS=SMSK,     FORMAT=A4 $
   FIELD=SMIN_SURQ,       ALIAS=SMSR,     FORMAT=A4.$
   FIELD=SCHAR_IMPD,      ALIAS=SIMP,     FORMAT=A4.$
   FIELD=SPULS_CLS,       ALIAS=SPLS,     FORMAT=A25 $
   FIELD=SPRF_RT,         ALIAS=SPRF,     FORMAT=A4.$
   FIELD=SPRF_%,          ALIAS=SPC,      FORMAT=A4.$
   FIELD=SRF_TIM_MN,      ALIAS=SRTN,     FORMAT=A4.$
   FIELD=SRF_TIM_MX,      ALIAS=SRTX,     FORMAT=A4.$
   FIELD=SWRD_LEN,        ALIAS=SWL,      FORMAT=A2.$
   FIELD=SBT_PTRQ,        ALIAS=SBTP,     FORMAT=A10.$
   FIELD=SSYNCHR,         ALIAS=SSYN,     FORMAT=A3.$
   FIELD=SSYN_WDTH,       ALIAS=SWD,      FORMAT=A4.$
   FIELD=STIME,           ALIAS=STM,      FORMAT=A4.$
   FIELD=SHZ,             ALIAS=SHZ,      FORMAT=A3.$
   FIELD=SIMPD,                           FORMAT=A4.$
   FIELD=PLOG0V,          ALIAS=PL0V,     FORMAT=A4.$
   FIELD=PLOG1V,          ALIAS=PL1V,     FORMAT=A4.$
   FIELD=PLOG0P,          ALIAS=PL0P,     FORMAT=A4.$
   FIELD=PLOG1P,          ALIAS=PL1P,     FORMAT=A4.$
   FIELD=PMIN_SNK,        ALIAS=PMSK,     FORMAT=A4.$
   FIELD=PMIN_SUR,        ALIAS=PMSR,     FORMAT=A4.$
   FIELD=PCHR_IMP,        ALIAS=PIMP,     FORMAT=A4.$
   FIELD=PPLS_CLS,        ALIAS=PPLS,     FORMAT=A25.$
   FIELD=PPRF_RT,         ALIAS=PPRF,     FORMAT=A4.$
   FIELD=PPRF_PC,         ALIAS=PPC,      FORMAT=A4.$
   FIELD=PRFTIMN,         ALIAS=PRTN,     FORMAT=A4.$
   FIELD=PRFTIMX,         ALIAS=PRTX,     FORMAT=A4.$
   FIELD=PWRD_LEN,        ALIAS=PWL,      FORMAT=A2.$
   FIELD=PBT_PTRN,        ALIAS=PBTP,     FORMAT=A10.$
   FIELD=PSYNCHR,         ALIAS=PSYN,     FORMAT=A3.$
   FIELD=PSYNWD,          ALIAS=PWD,      FORMAT=A4.$
   FIELD=PTME,            ALIAS=PTM,      FORMAT=A4.$
   FIELD=PSHZ,            ALIAS=PHZ,      FORMAT=A3.$
   FIELD=PIMPD,                           FORMAT=A4.$
   FIELD=NOWDRSEQ,        ALIAS=PNWS,     FORMAT=A3.$
SEGNAME=PRGM_CHR,PARENT=VENDSEG,SEGTYPE=S1.$
   FIELD=MOD_NAME,        ALIAS=MOD_NM,   FORMAT=A40.$
   FIELD=VENDOR_POC,      ALIAS=POC,      FORMAT=A30.$
   FIELD=PRGM_SPEC,       ALIAS=PS,       FORMAT=A1.$
   FIELD=PRGM_TITLE,      ALIAS=PT,       FORMAT=A30.$
   FIELD=PCLR_APPL,       ALIAS=PCA,      FORMAT=A8.$
SEGNAME=FUNC_CHR,PARENT=PRGM_CHR,SEGTYPE=S1.$
   FIELD=FUNC_SEQ,        ALIAS=FSEQ,     FORMAT=I2.$
   FIELD=CHARACT,         ALIAS=CHR,      FORMAT=A60.$
SEGNAME=USEDON,PARENT=PRGM_CHR,SEGTYPE=S1.$
   FIELD=SYS_EMP,                         FORMAT=A20.$
   FIELD=START_DATE,      ALIAS=SD,       FORMAT=I6YMD.$
   FIELD=END_DATE,        ALIAS=ED,       FORMAT=I6YMD.$
SEGNAME=MECONSID,PARENT=PRGM_CHR,SEGTYPE=U.$
   FIELD=HEGHT,           ALIAS=HT,       FORMAT=A5.$
```

Figure F-1

```
    FIELD=WDTH,           ALIAS=WD,        FORMAT=A5,$
    FIELD=LNTH,           ALIAS=LN,        FORMAT=A5,$
    FIELD=WIGHT,          ALIAS=WG,        FORMAT=A5,$
    FIELD=CONN_TYP,       ALIAS=CTYP,      FORMAT=A10,$
    FIELD=CVENDOR,        ALIAS=CVND,      FORMAT=A20,$
    FIELD=CVEND_PN,       ALIAS=CVPN,      FORMAT=A16,$
    FIELD=SEM_COMPAT,     ALIAS=SEM,       FORMAT=A1,$
    FIELD=SEM_SIZ,        ALIAS=SZ,        FORMAT=A1,$
    FIELD=MIL_STD,        ALIAS=MS,        FORMAT=A20,$
    FIELD=COOL_REQ,       ALIAS=CR,        FORMAT=A5,$
    FIELD=COOL_MECH1,     ALIAS=CM1,       FORMAT=A50,$
    FIELD=COOL_MECH2,     ALIAS=CM2,       FORMAT=A70,$
    FIELD=COVER,          ALIAS=CVR,       FORMAT=A1,$
    FIELD=COVERCHR1,      ALIAS=CVR1,      FORMAT=A40,$
    FIELD=COVERCHR2,      ALIAS=CVR2,      FORMAT=A70,$
    FIELD=VOLT_REQ1,      ALIAS=VR1,       FORMAT=A4,$
    FIELD=VOLT_REQ2,      ALIAS=VR2,       FORMAT=A4,$
    FIELD=VOLT_REQ3,      ALIAS=VR3,       FORMAT=A4,$
    FIELD=VOLT_%,         ALIAS=VP1,       FORMAT=A4,$
    FIELD=AMP_REQ1,       ALIAS=AR1,       FORMAT=A4,$
    FIELD=AMP_REQ2,       ALIAS=AR2,       FORMAT=A4,$
    FIELD=AMP_REQ3,       ALIAS=AR3,       FORMAT=A4,$
    FIELD=AMP_%,          ALIAS=ARP,       FORMAT=A4,$
    FIELD=TST_PT_NO,      ALIAS=TPN,       FORMAT=A11,$
    FIELD=STRES_MEAS,     ALIAS=TSMD,      FORMAT=A1,$
    FIELD=SENSORTYP,      ALIAS=SNRT,      FORMAT=A60,$
    FIELD=CHPMNTCH,       ALIAS=CMT,       FORMAT=A55,$
    FIELD=DVPKTCH1,       ALIAS=DPT1,      FORMAT=A55,$
    FIELD=DVPKTCH2,       ALIAS=DPT2,      FORMAT=A55,$
SEGNAME=CHP_SET,PARENT=VENDSEG,SEGTYPE=S1,$
    FIELD=SET_TCHN,       ALIAS=ST,        FORMAT=A8,$
    FIELD=CHP_FUNC,       ALIAS=CF,        FORMAT=A40,$
    FIELD=TCH_CLAS,       ALIAS=TC,        FORMAT=A60,$
    FIELD=DEV_TYP,        ALIAS=DT,        FORMAT=A40,$
SEGNAME=INTF_BUS,PARENT=VENDSEG,SEGTYPE=S1,$
    FIELD=INTFC,                           FORMAT=A25,$
    FIELD=COMP_INTOP,     ALIAS=CI,        FORMAT=A1,$
    FIELD=COMM1,                           FORMAT=A60,$
    FIELD=COMM2,                           FORMAT=A60,$
SEGNAME=BIT_SCHM,PARENT=VENDSEG,SEGTYPE=S1,$
    FIELD=TEST_SCHM,      ALIAS=BFTS,      FORMAT=A20,$
    FIELD=OCLK_MOD,       ALIAS=OM,        FORMAT=A1,$
    FIELD=OPROCOP,        ALIAS=OP,        FORMAT=A1,$
    FIELD=OPROCOPCR,      ALIAS=OPC,       FORMAT=A40,$
    FIELD=OPROCBF,        ALIAS=OPBF,      FORMAT=A1,$
    FIELD=OPROCBFCR,      ALIAS=OPBFCR,    FORMAT=A40,$
    FIELD=DPTTSCM,        ALIAS=DTS,       FORMAT=A70,$
SEGNAME=BIT_CHAR,PARENT=BIT_SCHM,SEGTYPE=S1,$
    FIELD=BIT_SEQ,                         FORMAT=I2,$
    FIELD=BIT_CHAR,                        FORMAT=A70,$
END
>>
```

Figure F-1 (cont'd)

```
FILEDEF VHS DISK VHS.DAT
SET MSG=OFF.PAUSE=OFF
-RUN
-BEGIN
-SET &PFKEY=' ';
-SET &AN=' ';
-SET &&MOD_FUNC='
-SET &&VENDOR='
-MAINMENU
-CRTCLEAR
-CRTFORM
-"</2 "
-"MODULE FUNCTION:<&&MOD_FUNC"
-"VENDOR:<&&VENDOR"
-CRTFORM
-"</2 "
-"MODULE FUNCTION:<D.&&MOD_FUNC"
-"VENDOR:<D.&&VENDOR"
-" "
-"IF THIS IS AN ERROR TYPE 'Y' <&AN>"
-IF &AN EQ 'Y' GOTO MAINMENU;
-WRITE VHS &&MOD_FUNC &&VENDOR
-TYPE RUNNING......
EX ATSL
-RUN
-TYPE LOADING.....1
RUN ATS1
-RUN
-TYPE LOADING.....2
RUN ATS2
-RUN
-TYPE LOADING.....3
RUN ATS3
-RUN
-CRTFORM LINE 16
-"           PRESS 'F3' TO EXIT"
-"           PRESS 'ENTER' TO CONTINUE"
-" "
-"<&AN>"
-GOTO MAINMENU
-EXIT
-RUN
>>0
```

Figure F-2

```
MODIFY FILE ATS
FIXFORM ON VHS MOD_FUNC X1 VENDOR
  MATCH MOD_FUNC VENDOR
    ON NOMATCH INCLUDE
    ON MATCH REJECT
DATA VIA FIDEL
END
>>
```

Figure F-2 (cont'd)

```
MODIFY FILE ATS
FIXFORM ON VHS MOD_FUNC/25 X1 VENDOR/25
  MATCH MOD_FUNC VENDOR
    ON NOMATCH INCLUDE
    ON MATCH/NOMATCH
      GOTO BEGIN
CASE BEGIN
ACTIVATE RETAIN MOD_FUNC VENDOR
  CRTFORM
                          <.W.B. WESTINGHOUSE <.C  <77 M1
                THIS SCREEN ADDS DATA TO THE ATS FILE"
"MODULE FUNCTION: <D.MOD_FUNC>"
  "VENDOR: <D.VENDOR>"

  "MODULE NAME: <T.MOD_NAME>"
  COMPUTE
    TNAME/A40=MOD_NAME;
  MATCH MOD_FUNC VENDOR MOD_NAME
    ON NOMATCH TYPE "ADDING NEW SEGMENT"
    ON MATCH TYPE "MODIFY MODE"
    ON MATCH COMPUTE
         MOD_NAME=MOD_NAME;
    ON MATCH/NOMATCH
  CRTFORM LINE 6
    "MODULE NAME: <D.MOD_NAME>"
    "VENDOR POC: <T.POC>"
    "PROGRAM SPECIFIC (Y/N): <T.PS>"
    "PROGRAM TITLE: <T.PT>"
    "PECULIAR APPLICATION: <T.PCA>"
    ON NOMATCH INCLUDE
    ON MATCH UPDATE POC PS PT PCA
  GOTO TXTSET
ENDCASE
CASE TXTSET
  COMPUTE
    PFKEY/A4='    ';
    TX1/A70=;
    TX2/A70=;
    TX3/A70=;
    TX4/A70=;
    TX5/A70=;
    K1=0;
    FUNC_SEQ=0;
  NEXT FUNC_SEQ
    ON NEXT GOTO FUNCSET
    ON NONEXT GOTO TXT
ENDCASE
CASE FUNCSET
  COMPUTE
    K1=K1+1;
    TX1=IF K1 EQ 1 THEN D.CHR;
    TX2=IF K1 EQ 2 THEN D.CHR;
    TX3=IF K1 EQ 3 THEN D.CHR;
    TX4=IF K1 EQ 4 THEN D.CHR;
    TX5=IF K1 EQ 5 THEN D.CHR;
  GOTO TXTSET
ENDCASE
CASE TXT
  COMPUTE
```

Figure F-2 (cont'd)

```
      FUNC_SEQ=FUNC_SEQ+1.
    IF PFKEY EQ 'PF05' THEN GOTO EMP.
    TYPE "F5 TO LEAVE TEXT"
    MATCH FUNC_SEQ
      ON NOMATCH TYPE "ADDING NEW TEXT"
      ON MATCH TYPE "MODIFING TEXT"
      ON MATCH/NOMATCH
    CRTFORM LINE 11
    "     FUNCTIONAL CHARACTERISTICS"
    "<T.CHR>"
    "  "
    "<D.TX1>"
    "<D.TX2>"
    "<D.TX3>"
    "<D.TX4>"
    "<D.TX5>"
    ON NOMATCH INCLUDE
    ON MATCH UPDATE CHR
    IF PFKEY EQ 'PF05' THEN GOTO EMP;
    GOTO TXT
ENDCASE
CASE EMP
    TYPE "'F6' TO EXIT SYSTEM EMPLOYED"
    IF PFKEY EQ 'PF06' THEN GOTO CONSD;
    CRTFORM LINE 8
      "SYS EMPLOYED: <T.SYS_EMP>"
    IF PFKEY EQ 'PF06' THEN GOTO CONSD;
    MATCH SYS_EMP
      ON MATCH TYPE "YOU ARE IN THE MODIFY MODE"
      ON MATCH COMPUTE
                SYS_EMP=D.SYS_EMP;
      ON MATCH/NOMATCH
    CRTFORM LINE 8
      "SYS EMPLOYED: <D.SYS_EMP>"
      "START DATE: <T.START_DATE                        END_DATE: <T.END_DATE>"
      ON NOMATCH INCLUDE
      ON MATCH UPDATE START_DATE END_DATE
    TYPE "'F6' TO EXIT SYSTEM EMPLOYED"
    IF PFKEY EQ 'PF06' THEN GOTO CONSD;
    GOTO EMP
ENDCASE
CASE CONSD
      MATCH MOD_FUNC VENDOR MOD_NAME
        ON MATCH TYPE "YOU ARE IN THE MODIFY MODE"
        ON MATCH CONTINUE TO HT
        ON MATCH/NOMATCH
CRTFORM LINE 1
"                           <.W.B. WESTINGHOUSE <.C."
"               THIS SCREEN ADDS DATA TO THE ATS FILE"
"  "
        "  "
        "MODULE FUNCTION: <D.MOD_FUNC>"
        "VENDOR: <D.VENDOR>"
        "  "
        "HEIGHT           <T.HT>   <35 WIDTH                  <T.WD>"
        "LENGTH           <T.LN>   <35 WEIGHT                 <T.WG>"
        "CONNECT TYPE     <T.CTYP> <35 VENDOR                 <T.CVND>"
        "VENDOR PN        <T.CVPN> <35 SEM COMPATIBLE (Y/N)   <T.SEM>"
        "SIZE             <T.SZ>   <35 MIL-STD      <T.MS>"
        "COOLING REQUIR   <T.CR>W  <35 COVERED (Y/N)          <T CVR>"
```

Figure F-2 (cont'd)

```
 COOLING MECHN    <T.CM1>
 <T.CM2>
 CHARACTERIZE COVER <T.CVR1>
 <T.CVR2>
 VOLTAGE REQUIREMENT       <35 CURRENT REQUIREMENT
<T.VR1>V <+3<T.VR2>V <+3<T.VR3>V <+3<T.VP1>%
<T.AR1>A <+3<T.AR2>A <+3<T.AR3>A <+3<T.ARP>%        <^1 PGDN
                        <.W.B.  WESTINGHOUSE < C.     <^1 PGUP
            THIS SCREEN ADDS DATA TO THE ATS FILE

 MODULE FUNCTION: <D.MOD_FUNC>
 VENDOR: <D.VENDOR>

 TEST POINT       <T.TPN>  <35 TIME STRS MEAS (Y/N) <T TSMD>
 SENSOR TYPES <T.SNRT>
 CHIP MOUNT TECH <T.CMT>
              DEVICE PACKAGING     (2 LINES)
 <T.DPT1>
 <T.DPT2>
ON MATCH UPDATE HT WD LN WG CTYP CVND CVPN SEM SZ MS CR CM1 CM2 CVR
ON MATCH UPDATE CVR1 CVR2 VR1 AR1 VR2 AR2 VR3 AR3 VP1 ARP TPN TSMD
ON MATCH UPDATE SNRT CMT DPT1 DPT2
ON NOMATCH INCLUDE
GOTO EXIT
ENDCASE
DATA VIA FIDEL
END
>>
```

Figure F-2 (cont'd)

```
MODIFY FILE ATS
  COMPUTE
    PFKEY/A4='      ';
FIXFORM ON VHS MOD_FUNC X1 VENDOR
  MATCH MOD_FUNC VENDOR
    ON NOMATCH INCLUDE
    ON MATCH/NOMATCH
      GOTO BEGIN
CASE BEGIN
COMPUTE
  ST='       ';
CRTFORM
"                    <.W.B. WESTINGHOUSE <.CLEAR. <77 M2
                THIS SCREEN ADDS DATA TO THE ATS FILE"
" MODULE FUNCTION: <D.MOD_FUNC>"
" VENDOR: <D.VENDOR>"
"
     "CHIP SET TECHNOLOGY: <T.ST>"
   TYPE "'F5' TO GO TO INTERFACE"
   IF PFKEY EQ 'PF05' THEN GOTO FACE;
   MATCH MOD_FUNC VENDOR SET_TCHN
     ON MATCH TYPE "YOU ARE IN MODIFY MODE"
     ON MATCH COMPUTE
                ST=D.ST;
     ON MATCH/NOMATCH
   CRTFORM LINE 7
     "CHIP SET TECHNOLOGY: <D.ST>"
     "CHIP FUNCTION: <T.CF>"
     "TECHN CLASS: <T.TCH_CLAS>"
     "DEVICE TYPE: <T.DT>"
     ON NOMATCH INCLUDE
     ON MATCH UPDATE CF TCH_CLAS DT
   IF PFKEY EQ 'PF05' THEN GOTO FACE;
   GOTO BEGIN
ENDCASE
CASE FACE
   IF PFKEY EQ 'PF06' THEN GOTO EXIT;
   CRTFORM LINE 7
     "MODULE INTERFACE BUS: <T.INTFC>"
   MATCH MOD_FUNC VENDOR INTFC
     ON MATCH TYPE "YOU ARE IN MODIFY MODE"
     ON MATCH COMPUTE
                INTFC=D.INTFC;
     ON NOMATCH TYPE "YOU'RE IN ADD MODE"
     ON MATCH/NOMATCH
   CRTFORM LINE 7
     "MODULE INTERFACE BUS: <D.INTFC>"
     "BUS COMPLIANT W/ INTEROPERABILITY SPEC (Y/N):<T.COMP_INTOP>"
     "COMMENT (DEVIATIONS FORM SPEC)     UP TO 2 LINES"
     "<T.COMM1>"
     "<T.COMM2>"
     ON MATCH VALIDATE
       GTEST=COMP_INTOP EQ 'Y' OR COMP_INTOP EQ 'N';
     ON INVALID TYPE
       "MUST BE 'Y' OR 'N'"
     ON INVALID GOTO FACE
     ON NOMATCH VALIDATE
       GTEST=COMP_INTOP EQ 'Y' OR COMP_INTOP EQ 'N';
```

Figure F-2 (cont'd)

```
    ON INVALID TYPE
        MUST BE 'Y' OR 'N'
    ON INVALID GOTO FACE
    ON NOMATCH INCLUDE
    ON MATCH UPDATE COMP_INTOP COMM1 COMM2
  TYPE  'F6' TO EXIT INTERFACE
  IF PFKEY EQ 'PF06' THEN GOTO EXIT
  GOTO FACE
ENDCASE
DATA VIA FIDEL
END
>>
```

Figure F-2 (cont'd)

```
MODIFY FILE ATS
  COMPUTE
    PFKEY A4=
FIXFORM ON VHS MOD_FUNC X1 VENDOR
  MATCH MOD_FUNC VENDOR
    ON NOMATCH TYPE  <D VENDOR IS A NEW VENDOR
    ON MATCH NOMATCH CRTFORM
                                    < W B  WESTINGHOUSE <  CLEAR  <77 M3
                         THIS SCREEN ADDS OR MODIFIES DATA TO THE ATS DATABASE
   MODULE FUNCTION  <D MOD_FUNC>
   VENDOR            <D VENDOR>

                              SERIAL DATA STIMULI
   LOGIC 0 VT        <T SLOV>V        <39 LOGIC 0 %         <T SLOP>
   LOGIC 1 VT        <T SL1V>V        <39 LOGIC 1 %         <T SL1P>
   MIN SINK          <T SMSK>MA       <39 SOURCE REQ        <T SMSR>MA
   CHAR IMPED        <T SIMP>OHMS     <39 PULSE CLASS <T SPLS>
   BIT PRF           <T SPRF>MHZ      <39 BIT PRF            <T SPC>%
   BIT RISE (MIN)    <T SRTN>         <39 BIT RISE (MAX)    <T SRTX>
   WORD LENGTH       <T SWL>BITS      <39 PATTERN            <T SBTP>
   SYNC REQUIRE      <T SSYN>V        <39 WIDTH             <T SWD>SECONDS
   RISE/FALL TIME <T STM>SECONDS <39 PRF                     <T SHZ>HZ
   IMPEDANCE         <T SIMPD>OHMS
    <2
   <71 MORE
                                   < W B  WESTINGHOUSE <  CLEAR
                         THIS SCREEN ADDS OR MODIFIES DATA TO THE ATS DATABASE
   MODULE FUNCTION  <D MOD_FUNC>
   VENDOR            <D VENDOR>

                           PARALLEL DATA STIMULI  <72 UP
   LOGIC 0 VT        <T PLOV>         <39 LOGIC 0 %          <T PLOP>
   LOGIC 1 VT        <T PL1V>         <39 LOGIC 1 %          <T PL1P>
   MIN SINK          <T PMSK>MA       <39 SOURCE REQ         <T PMSR>MA
   CHAR IMPED        <T PIMP>OHMS     <39 PULSE CLASS <T PPLS>
   BIT PRF           <T PPRF>MHZ      <39 BIT PRF             <T PPC>%
   BIT RISE (MIN) <T PRTN>            <39 BIT RISE (MAX)   <T PRTX>
   WORD LENGTH       <T PWL>  BITS    <39 PATTERN              <T PBTP>
   SYNC REQUIRE      <T PSYN> V       <39 WIDTH               <T PWD>SECONDS
   RISE/FALL TIME <T PTM>SECONDS <39 PRF                       <T PHZ> HZ
   IMPEDANCE         <T PIMPD>OHMS    <39 NO. WRD SEQ.      <T PNWS>
    ON NOMATCH INCLUDE
    ON MATCH UPDATE SLOV SLOP SL1V SL1P SMSK SMSR SIMP SPLS SPRF SPC
    ON MATCH UPDATE SRTN SRTX SWL SBTP SSYN SWD STM SHZ SIMPD
    ON MATCH UPDATE PLOV PLOP PL1V PL1P PMSK PMSR PIMP PPLS PPRF PPC
    ON MATCH UPDATE PRTN PRTX PWL PBTP PSYN PWD PTM PHZ PIMPD PNWS
  GOTO BIT
CASE BIT
  TYPE  PRESS 'F5' TO LEAVE TESTABILITY SCHEME"
  IF PFKEY EQ 'PF05' THEN GOTO BITCHK.
  COMPUTE
    TS1/A70=' '.
    TS2/A70=' '.
    TS3/A70=' '.
    BFTS1/I2=.
    BFTS2/I2=.
    BFTS3/I2=.
    K1/I1=0.
  CRTFORM LINE 5
```

Figure F-2 (cont'd)

```
 TESTABILITY SCHEME  <T BFTS
MATCH MOD_FUNC VENDOR BFTS
  ON MATCH TYPE  YOU ARE IN MODIFY MODE
  ON MATCH NOMATCH
CRTFORM LINE 5

 ON-MOD CLOCK (Y/N)  <T OM>
 ON-MOD PROCESSOR FOR OPERATIONAL USE  Y N   T  P
 CHARACTERIZE <T OPC>
 ON-MOD PROCESSOR FOR BIT/FIT USE  Y N   T  PBF
 CHARACTERIZE <T OPBFCR>
 <20 PROJECTED DEPOT TEST SET COMPATIBILITY
 <T DTS>
  ON MATCH VALIDATE
    GTEST=OM EQ 'Y' OR 'N' OR ' '.
  ON INVALID TYPE
     ON-MOD CLOCK MUST BE  Y' OR  N'
  ON INVALID GOTO BIT
  ON NOMATCH VALIDATE
    GTEST=OM EQ 'Y' OR 'N' OR ' '.
  ON INVALID TYPE
     ON-MOD CLOCK MUST BE 'Y' OR N
  ON INVALID GOTO BIT
  ON NOMATCH VALIDATE
    GTEST=OP EQ 'Y' OR 'N' OR ' '.
  ON INVALID TYPE
     ON-MOD PROCESSOR FOR OPS USE MUST BE 'Y' OR 'N'
  ON INVALID GOTO BIT
  ON MATCH VALIDATE
    GTEST=OP EQ 'Y' OR 'N' OR ' '.
  ON INVALID TYPE
     ON-MOD PROCESSOR FOR OPS USE MUST BE 'Y' OR 'N'
  ON INVALID GOTO BIT
  ON NOMATCH VALIDATE
    GTEST=OPBF EQ 'Y' OR 'N' OR ' '.
  ON INVALID TYPE
     ON-MOD PROCESSOR FOR BIT/FIT MUST BE 'Y' OR 'N'
  ON INVALID GOTO BIT
  ON MATCH VALIDATE
    GTEST=OPBF EQ 'Y' OR 'N' OR ' '.
  ON INVALID TYPE
     ON-MOD PROCESSOR FOR BIT/FIT MUST BE 'Y' OR 'N'
  ON INVALID GOTO BIT
  ON NOMATCH INCLUDE
  ON MATCH UPDATE OM OP OPBF DTS
  COMPUTE
    K1=0;
 IF PFKEY EQ 'PF05' THEN GOTO BITCHK;
 GOTO BIT
ENDCASE
CASE BITCHK
 IF K1 EQ 4 THEN GOTO BITCHR;
 NEXT BIT_SEQ
  ON NEXT COMPUTE
    K1=K1+1;
  TS1=IF K1 EQ 1 THEN D.BIT_CHAR;
  BFTS1=IF K1 EQ 1 THEN BIT_SEQ;
  TS2=IF K1 EQ 2 THEN D.BIT_CHAR;
  BFTS2=IF K1 EQ 2 THEN BIT_SEQ;
  TS3=IF K1 EQ 3 THEN D.BIT_CHAR;
```

Figure F-2 (cont'd)

```
    BFTS3::IF K1 EQ 3 THEN BIT_SEQ
    ON NEXT GOTO BITCHK
    ON NONEXT COMPUTE
                 BIT_SEQ=1
    ON NONEXT GOTO BITCHR
ENDCASE
CASE BITCHR
  TYPE  PRESS 'F5' TO LEAVE
  MATCH BIT_SEQ
    ON NOMATCH TYPE  ADDING TEXT
    ON MATCH TYPE  MODIFING TEXT
    ON MATCH NOMATCH
  CRTFORM LINE 5
   <20 ELABORATE
   <T BIT_CHAR>

   1 <D TS1>
   2 <D TS2>
   3 <D TS3>
    ON NOMATCH INCLUDE
    ON MATCH UPDATE BIT_CHAR
  IF PFKEY EQ 'PF05' THEN GOTO TOP.
  COMPUTE
    BIT_SEQ=BIT_SEQ+1.
  GOTO BITCHR
ENDCASE
DATA VIA FIDEL
END
>>
```

Figure F-2 (cont'd)

F. Data Base Hierarchy

Refer to Figure F-3

G. Questionnaire

Figure F-4 outlines the study questionnaire with associated input variable.

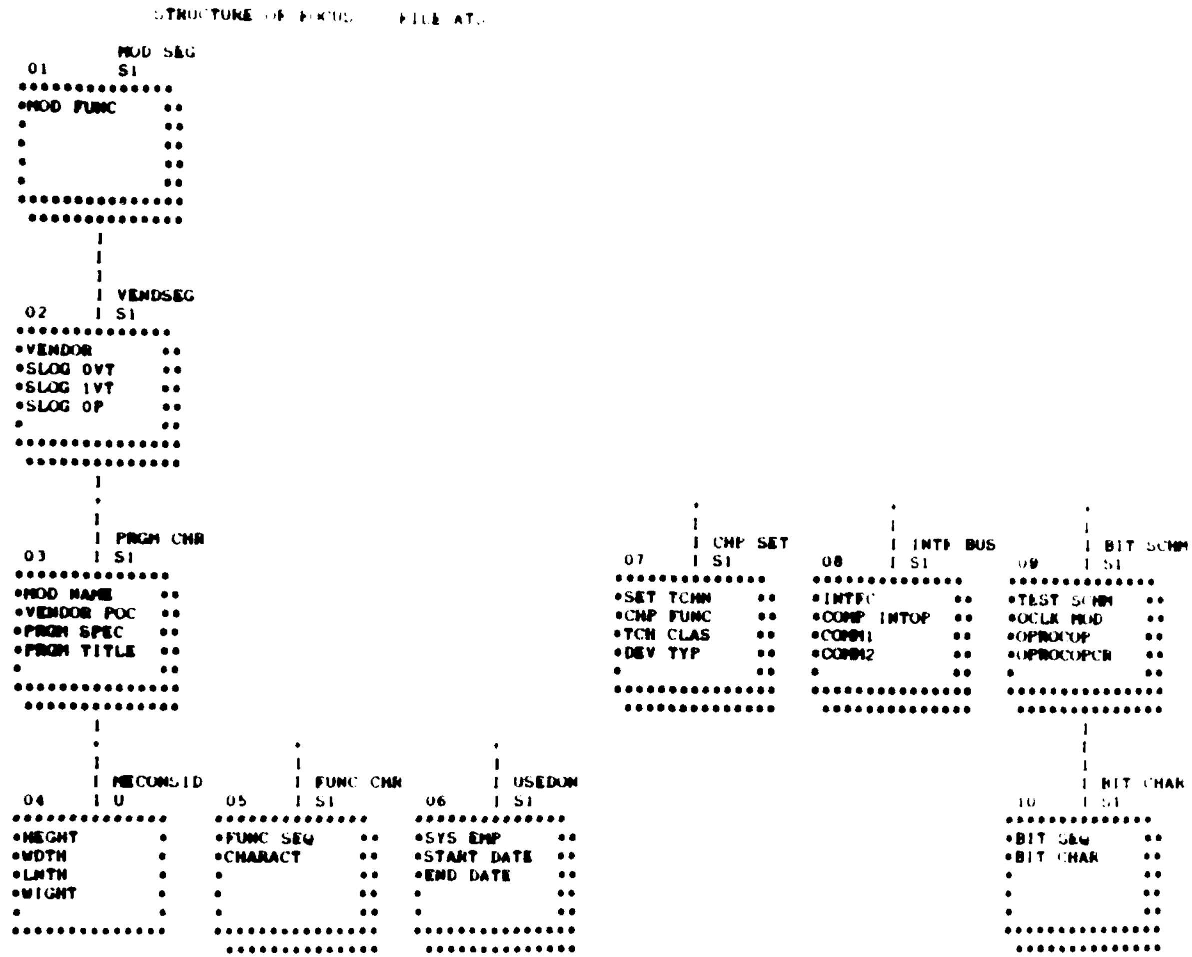

Figure F-[illegible]. Data Base Hierarchy

WESTINGHOUSE

VHSIC/ATS VENDOR SURVEY

MODULE CHARACTERIZATION:

Vendor - VENDOR

Vendor Point of Contact, Title - VENDOR POC

Module Name - MOD NAME

Module Function (1750A, BMM, FFT,...) - MOD FUNC

Functional Characteristics (ie. MIPS, process rate, local memory size, programming language, redundancy characteristics,...) - CHARACT

- PRGM_SPEC

Program Specific (Y/N)___ If yes, Program Title - PRGM TITLE

Peculiar/Common Application - PCLR APPL

Projected

System(s) to employ this module - SYS EMP Start Date - START DATE

End Date - END DATE

Start Date

End Date

Start Date

End Date

Start Date

End Date

Figure F-4

Chip Set Technologies employed for all functional components:
- SET_TCHN

Phase I VHSIC (y/n) ___ **If yes, Chip Function(s)** - CHP FUNC ______

Technology Classification - TCH CLAS ______

Device Type (ie. CPU, X-Bar, RAM, ROM,...) - DEV TYP ______

Phase II VHSIC (y/n) ___ **If yes, Chip Function(s)** ______

Classification (ie. nK Gate Array, Custom, Semi-Custom,...) ______

Device Type (ie. CPU, X-Bar, RAM, ROM,...) ______

VLSI (y/n) ___ **If yes, Chip Function(s)** ______

Classification ______

Device Type ______

Bipolar (y/n) ___ **If yes, Chip Function(s)** ______

Classification ______

Device Type ______

GaAs (y/n) ___ **If yes, Chip Function(s)** ______

Classification ______

Device Type ______

CMOS (y/n) ___ **If yes, Chip Function(s)** ______

Classification ______

Device Type ______

NMOS (y/n) ___ **If yes, Chip Function(s)** ______

Classification ______

Device Type ______

SOS (y/n) ___ **If yes, Chip Function(s)** ______

Classification ______

Device Type ______

Figure F-4 (cont'd)

TTL (y/n) __ If yes, Chip Function(s) ____________________

Classification ____________________

Device Type ____________________

- SET_TCHN

Other (y/n) __ If yes, Chip Function(s) - CHP FUNC

Classification - TCH CLAS

Device Type - DEV TYP

Module To Module Interface Bus:

NOTE: COPIES OF APPLICABLE INTEROPERABILITY SPECIFICATIONS ATTACHED.

- INTFC

Parallel Interface Bus (Y/N) ____ Bus Compliant with Interoperability Specification (Y/N) ___ Comment (deviations from spec) - COMM1 & 2

- COMP INTOP

- INTFC

Test/Maintenance Bus (Y/N) ____ Bus Compliant with Interoperability Specification (Y/N) ___ Comment (deviations from spec) -COMM1 & 2

- COMP INTOP

Extended T/M (ETM) Bus (Y/N) ____ Bus Compliant with Interoperability Specification (Y/N) ___ Comment (deviations from spec) ____________________

Fiber Optic HSDB (Y/N) ____ Bus Compliant with Interoperability Specification (Y/N) ___ Comment (deviations from spec) ____________________

Other Bus architectures applicable to advanced systems ____________________

Figure F-4 (cont'd)

Serial data stimuli:

- SLOG_0VT -L LOG_0P -SLOG_1VT -SLOG_1P

Logic "0"/"1" voltages ___.0V +/-____% ___.0V +/- %

Minimum current sink/source requirements - SMIN SNK - SMIN SURQ

Characteristic Impedance - SCHAR IMPD

Pulse Class (RZ, NRZ,...) - SPULS

Bit prf (clock rate) - SPRF RT - SPRF_%

Bit rise and fall time (min/max) - SRF TIM MN / - SRF TIM_MX

Word Length - SWRD LEN Pattern of Bits required - SBT PTRQ

Synchronization requirements (reference signal from UUT) amplitud- SSYNCHR

width: - SSTN WDTH rise/fall time: - STIME Prf: - SHZ

Impedance: - SIMPD

Parallel data stimuli:

- PLOG0V - PLOG0P - PLOG1V - PLOG1P

Logic "0"/"1" voltages ___.0V +/-____% ___.0V +/- %

Minimum current sink/source requirements ________A ________A

Characteristic Impedance - PCHR IMP

Pulse Class (RZ, NRZ,...) - PPLS CLS

Bit prf (clock rate) - PPRF RT - PPRF_PC

Bit rise and fall time (min/max) - PRFTIMN - PRFTIMX

Word Length - PWRD LEN Pattern of Bits required - PBT PTRN

Synchronization requirements (reference signal from UUT) amplitu - PSYNCHR

width: - PSYNWD rise/fall time: - PTME Prf: - PSHZ

Impedance: - PIMPD

Number of Words in sequence - NOWDRSEQ

Figure F-4 (cont'd)

BIT/FIT Scheme: - TEST_SCHM

Testability scheme (Level Sensitive Scan Design, Boundary Scan, Built in Self Test with BILBO, Signature Analysis, Pseudo Random TPG on chip,...) please elaborate:
- BIT CHAR

On-module clock (Y/N) - OCLK_MOD

-OPROCOP

On-module Processor for operational use (Y/N) ___ If yes, characterize (including programming languages) - OPROCOPCR

- OPROCBF

On-module Processor for BIT/FIT use (Y/N) ___ If yes, characterize (including programming languages, bus interfaces, architecture) ______
- OPROCBFCR

Projected depot test set compatibility (ie, DATSA, 320, 390,...) ______
- DPTTSCM

Figure F-4 (cont'd)

Mechanical/Electrical Considerations:

Module Dimensions H - HEGHT W - WDTH L - LNTH

Weight - WIGHT

Connector Type - CONN TYP Vendor - CVENDOR

Vendor PN - CVEND PN

- SEM_COMPAT

Standard Electronic Module (SEM) Compatible (Y/N) ___ If yes, which size (A, B, C, D, E...) ___ Applicable Mil Stds/Specs being used to guide design - MIL STD - SEM SIZ

Cooling Requirement (Power to dissipate) - COOL REQ

Cooling Mechanism - COOL MECH1

- COOL MECH2

- COVER

Is module covered (Y/N) If yes, characterize cover - COVERCHR1

- COVERCHR2

Input Voltage Requirement(s) - VOLT REQ1 Q2 Q3 - VOLT %

Current Requirement(s) - AMP REQ1 Q2 Q3 - AMP %

Test Point scheme (no. and access) - TST PT NO

- STRES_MEAS

Time Stress Measurement Devices on-module (Y/N) ___ Sensor Types ___

- SENORTYP

Chip mounting technique(s) - CHPMNTCH

Device Packaging technique(s) - DVPKTCH1

- DVPKTCH2

Figure F-4 (cont'd)

Additional Comments

Figure F-4 (cont'd)

APPENDIX G

Tester Independent Support Software (TISSS)/
VHSIC Hardware Descriptive Language (VDL)

Tester Independent Support Software System (TISSS)

The primary purpose of the Tester Independent Support Software System (TISSS) is to integrate and automate the generation of complex test specifications. TISSS which is under development by the Harris Corporation will dramatically affect system(s) life cycle cost through the maintenance of test specifications and test program sets for rapidly evolving VHSIC digital devices and boards. TISSS is a critical element of VHSIC automatic test systems and is in consonance with the MASA AFR 800-45.

Background

TISSS is based on four concepts: the establishment of a standard, machine readable, tester-independent test specification format for microcircuits; automated use of design information for test specification generation; automatic generation of test specifications; and, the automated generation and maintenance of test programs. TISSS relies on the establishment of the MASA unified data base (UDB) as an input member to test program upgrading.

Standardized formats will be critical to the implementation of automated, tester independent, test specifications. The standard format will replace the hardcopy Mil-M-38510 Detail Specification format now in use. Chip/board design parameters, simulations, and timing analyses will be extracted from vendor Computer Aided Engineering (CAE)/Computer Aided Design (CAD) systems and will automatically serve as the substance of a standard test specification.

The standard test specification will allow for the automatic generation of test programs. As such, Test programs will have their origins in the vendor CAE/CAD system where the circuit was simulated and validated. Test specifications and subsequent test programs will be automatically updated through a network as chip/board designs are modified.

A critical element of the MASA Air Force Regulation is a depot/vendor feedback network. The TISSS network will allow for two-way communication: Vendor CAE/CAD data will be transferred through the TISSS network; and, failure data which includes environmental overstresses will be relayed back to the vendor via the Unified Data Base. Failure trend analysis with subsequent design modifications and/or test modifications will automatically be available to the depot. In addition to test specification/test program management, the TISSS/UDB will serve to enhance system reliability.

TISSS Architecture

VHSIC Automatic Test Systems will exploit the TISSS interface between the circuit designer and the depot test technician. Elements of the TISSS architecture that must be addressed by the VHSIC/ATS architecture include: the TISSS Pre-processor; the TISSS Input Format (TIF); the Design Input level; the internal audit cycle; the Modeling Subsystem; the TISSS Output Format; and, the TISSS Post-processor (refer to figure G-1).

TISSS ARCHITECTURE

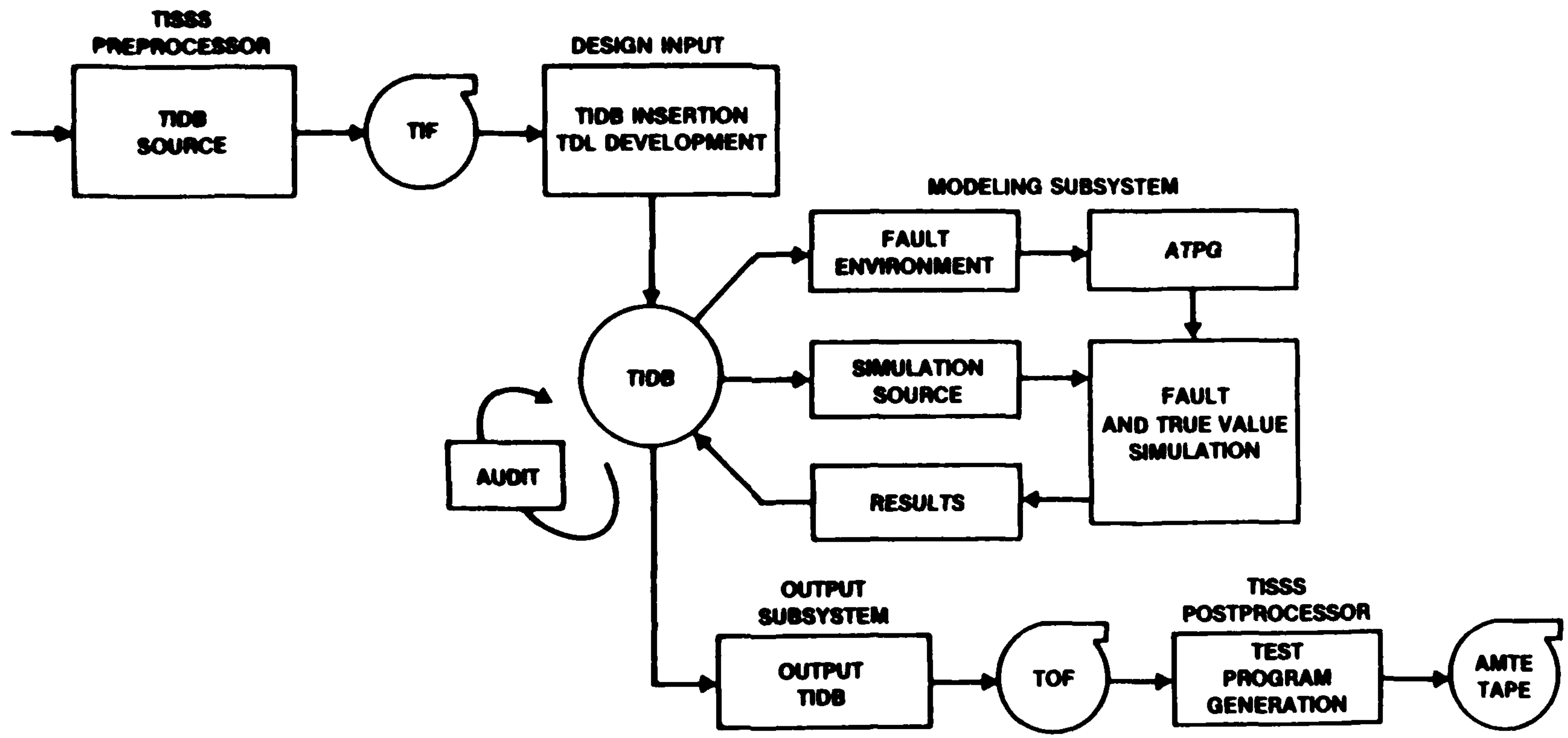

Figure G-1

TISSS Pre-processor. The TISSS Pre-processor serves to extract and format design/test information from the vendor CAE/CAD tool set into the standard TISSS Input Format (TIF). TIF is standardized around Mil-M-38510 detail specification requirements. Pulled from the vendor CAE/CAD data base is textural information required to satisfy Mil-M-38510 and product specifications. The TIF will include a directory, Electronic Design Interchange Format (EDIF) graphical information, test philosophy, and circuit simulation models and vector sets. Vector sets will be standardized in Test Vector Language (TVL) which is a VHSIC hardware descriptive language (VHDL) subset.

Design Input. The Design Input element of the TISSS accepts formatted CAE/CAE data from the Pre-processor into the TISSS data base. Specific Ada based Test Descriptive Language (TDL) is generated in the Design Input stage in addition to TIF verification.

Modeling Subsystem. The Modeling Subsystem provides the set of tools that accept and perform true value and fault simulations. Automatic generation of stimuli for combinational circuits is developed at this stage. In tandem with the audit stage, test programs will be assessed and validated through simulation before a validated vector set is downloaded to the ATS.

Audit Stage. As the name implies, the audit stage is an iterative process that provides a set of analysis and verification tools. It serves to validate TISSS data base data sets. Administrative management or configuration control is a key element of the audit stage.

<u>Output Subsystem.</u> The Output Subsystem extracts machine-readable detailed specifications from the TISSS data base and formats the data into TISSS Output Format (TOF). TOF is a a subset of the TIF consisting of the test plan and its referenced items to the full TIF. TOF coontents will preclude vendor proprietary data; subsequently, the contents of the TOF will be based on manual operator intervention.

<u>Post-processor.</u> The Post-processor is responsible for automatic test program generation (ATPG) of test programs using the TOF files and parametric test macros. The Post-processor will generate formatted test specifications.

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This effort defineed the automatic testing requirement for VHSIC based system modules lending to the development of an automatic test system (ATS) architecture. The technologies needed to initiate the development of an ATS for VHSIC Based systems and the characteristics of the expected population of VHSIC modules that will be developed over the next ten years were identified.

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